PIE Tech

POLLACHI INSTITUTE OF ENGINEERING AND TECHNOLOGY

(Approved by AICTE and Affiliated to Anna University)

sky is the limit

Department of Electrical and Electronics Engineering

Regulation 2021

II Year – III Semester

EC3301- Electronics Circuits and Devices

UNIT- I
PN JUNCTION DIODE

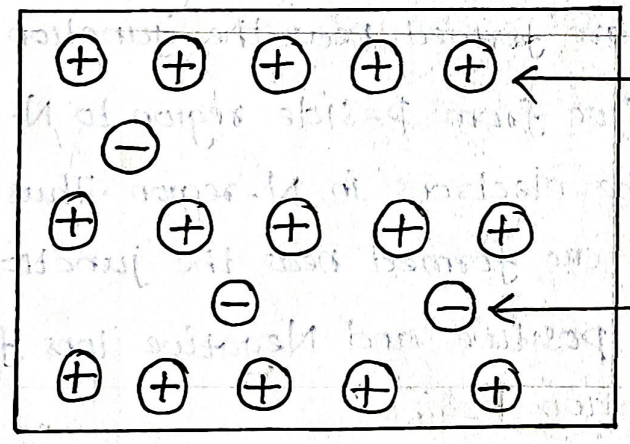
In a piece of Semiconductor, one half is doped by P-type Impurity and the other half is doped by N-type Impurity. Thus PN Junction is formed.

- This formation of PN junction is called diode as it has two electrodes - one for P-Region called as 'Anode' and the other for N-Region called as 'Cathode'

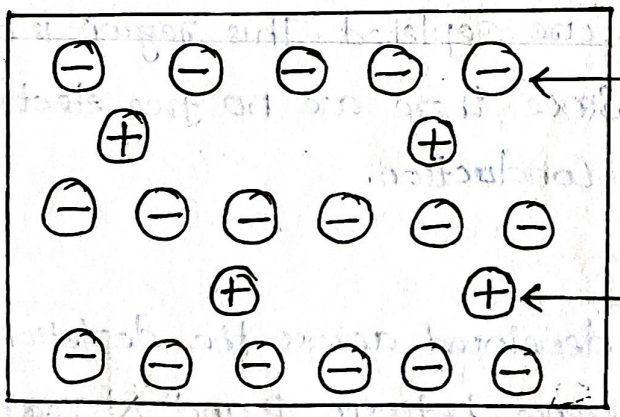
N-TYPE MATERIAL & P-TYPE MATERIAL

The majority charge carriers are electrons and N-type has higher Concentration of free electrons than holes as shown in fig. 1 (a).

- The Majority Charge Carriers are holes and P-type material has higher Concentration of holes than electrons as shown in fig. 1 (b).



a) P-Type



b) N-Type

Fig. 1. P-Type and N-Type Material

DIFFUSION :

The tendency of the free electrons to diffuse from N-side to p-side and holes from p-region to N-region is called 'diffusion'

- Diffusion is the process by which charge carrier moves from high concentration region to Low concentration region.

DEPLETION REGION :

The free electrons diffuse from 'n'-side to 'p'-side region and recombine with the holes in P-region. Thus

- Also, the holes diffuse from P-side region to N-side region and recombine with the electrons in

DEPLETION REGION :

The free electrons diffuse from n-side to P-side region and recombine with the holes in P-region. Thus Negative charged immobile ions are formed near the junction of P-side

- Also the holes diffuse from p-side region to N-side region and recombine with the electrons in N-region. Thus positive charged immobile ions are formed near the junction of N-side

* These immobile positive and Negative ions form a region called as "depletion Region"

Depletion region is defined as the region over which all the free charge carriers are depleted. This region is also known as "Space charge Region" since there are no free ~~electrons~~ charge carriers available for conduction.

BARRIER POTENTIAL :

The electric field is developed across the depletion region due to the potential difference between P and N regions

This potential act as barrier for further conduction between the junctions. This potential is called as "barrier potential" or diffusion potential or Contact potential or "Cut in Voltage"

* It depends on doping levels and Temperature
* The Value of Contact potential is 0.3V for Germanium and 0.7V for Silicon at 25°C.

The barrier potential depends on

- The type of Semiconductors
- Concentration of donar impurity on n-side
- Concentration of Acceptor Impurity on p-side
- Intrinsic Concentration of Semiconductors
- Temperature.

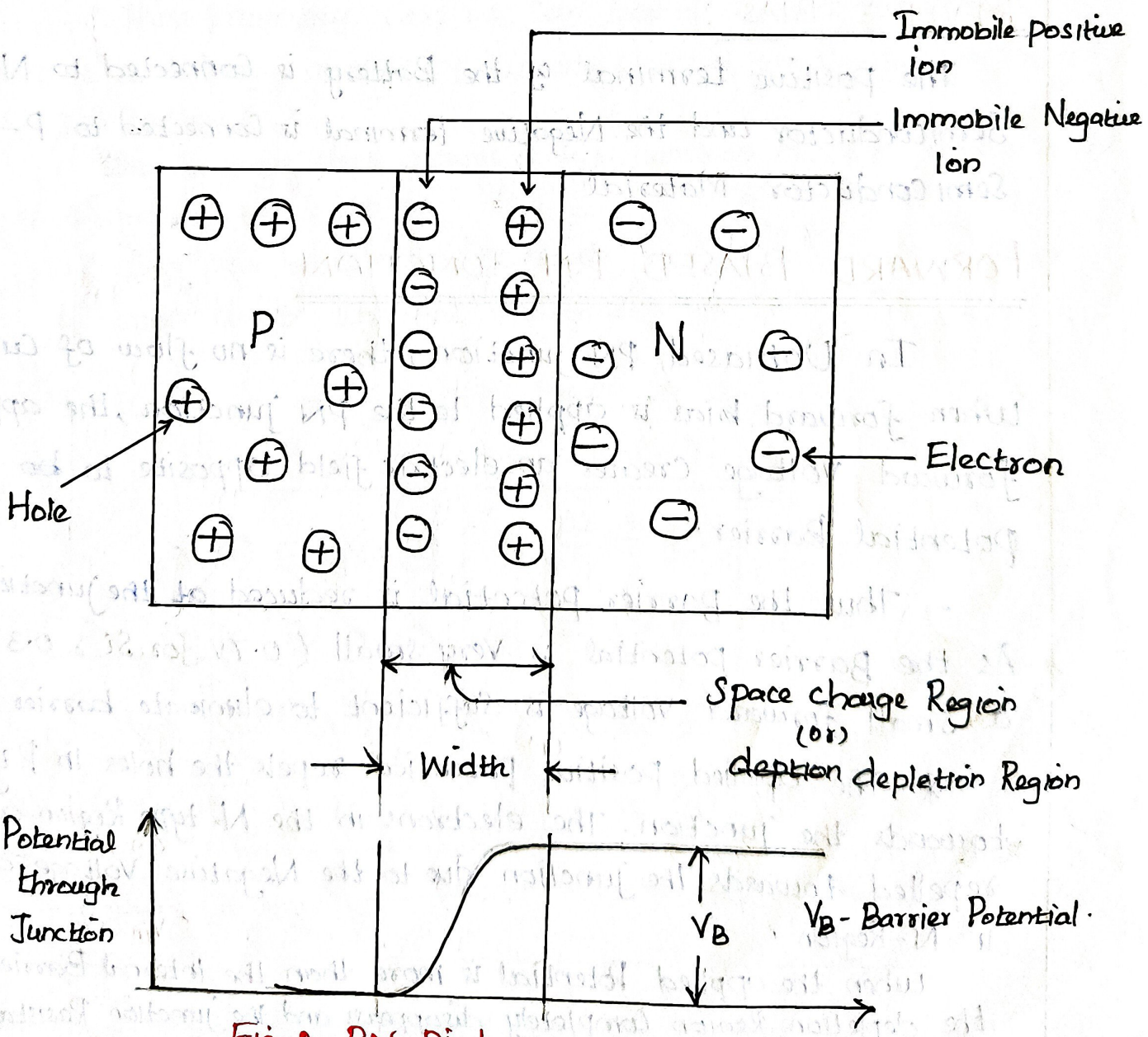


Fig. 2. PN Diode.

OPERATION OF PN JUNCTION DIODE

BIASING :

Applying any External Voltage to electronic device is called 'Biasing'. Biasing refers to provide Minimum External Voltage and Current to activate the device.

- There are two types of biasing for PN junction

FORWARD BIAS :

The positive terminal of the Battery is Connected to P-type Semiconductor and Negative Terminal is Connected to N-type Semiconductor material

REVERSE BIAS :

The positive terminal of the Battery is Connected to N-type Semiconductor and the Negative Terminal is Connected to P-type Semiconductor Material.

FORWARD BIASED PN JUNCTION

In Unbiased PN junction, there is no flow of Current, When forward bias is applied to the PN junction, the applied forward Voltage Creates an electric field opposite to ~~to~~ the potential Barrier.

- Thus the Barrier potential is reduced at the junction. As the Barrier potential is very small (0.7V for Si & 0.3V for Ge), a Small forward Voltage is Sufficient to eliminate barrier Potential.

* The applied positive (+) potential repels the holes in P-type Region towards the junction. The electrons in the N-type Region are also repelled towards the junction due to the Negative (-) Voltage applied in N-Region.

$V_{in} > V_B$

When the applied Potential is more than the Internal Barrier Potential the depletion Region Completely disappears and the junction Resistance becomes zero. ($R=0$)

The junction provides a Low Resistance path and thus current flows in the circuit. This current is called 'forward current' I_f

– When the forward voltage is increased, the large Number of Majority charge carriers can cross the junction. These large Number of Majority charge carriers constitute the 'forward current'.

Hole Current:

The current in P-region is due to the movement of holes which are Majority carriers. This is called 'hole current'

Electron Current:

The current in N-region is due to the movement of free electrons which are majority carriers. This is called 'Electron current'.

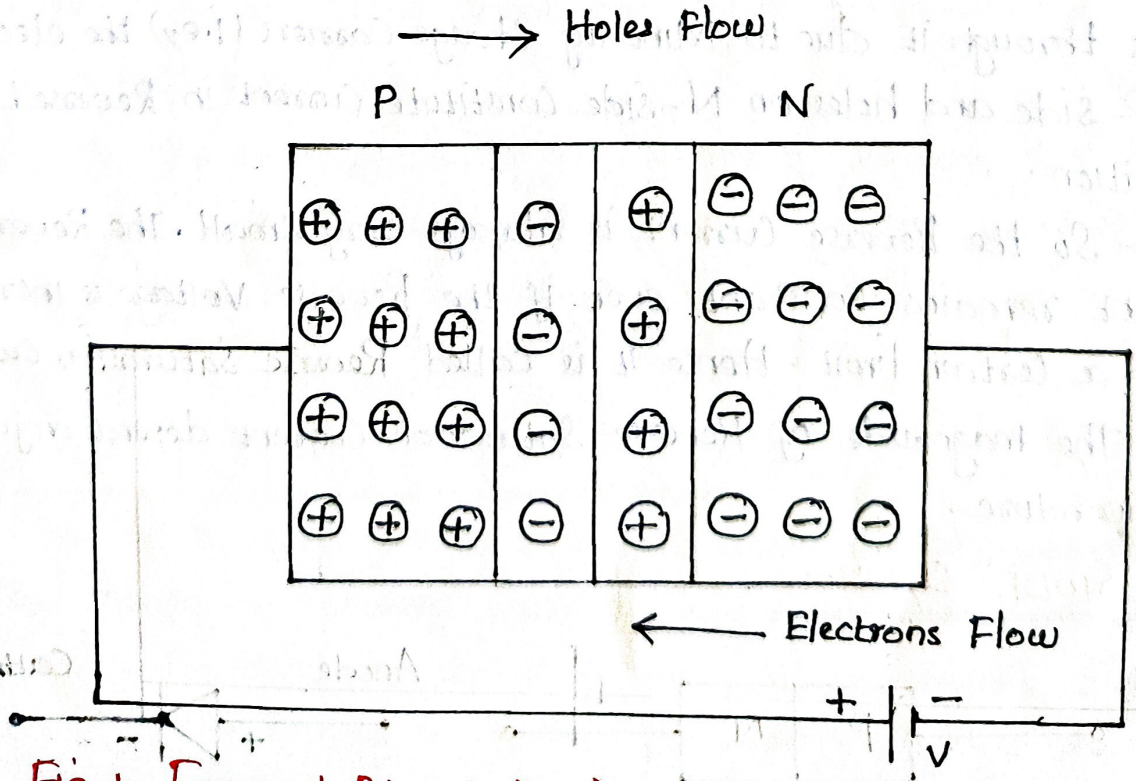
The Overall forward current is due to the Majority charge carriers.

* These majority carriers can travel around the closed circuit and large amount of current flows from Negative to positive of the battery.

– The voltage drop across a P-N junction diode in forward biased condition is made up of

i) drop due to barrier Potential

ii) drop due to Internal Resistance.



Fig·1 Forward Biased PN junction

REVERSE BIASED P-N JUNCTION

The P-region is Connected to Negative terminal of the Battery and N-region is Connected to Positive terminal of the Battery.

- When P-N junction is Reverse biased, the Negative terminal attracts the holes in P-region and the Positive terminal attracts the Free electrons in N-region away from the junction

* The electrons and holes move away from the junction and the Width of depletion region Increases. the Charge Carriers are Unable to Cross the junction.

Thus there are more positive ions in the N-region and more Negative ions in the P-region. When the depletion region widens, the barrier potential across the junction also increases

- The applied Reverse Voltage Creates an electric field which is in Same direction of barrier potential and thus Barrier Width is Increased. This Increased barrier potential prevents the flow of Charge Carriers across the junction.

* When PN junction is reverse biased, it has high Resistance Path and No Current flows in the Circuit. After Certain extent, the 'junction Breakdown' occurs. Then a small amount of current flows through it due to Minority Charge Carriers (i.e,) the electrons on P-side and holes on N-side Constitute Current in Reverse biased Condition.

- So the Reverse Current is always very small. The Reverse Current remains Constant even if the Reverse Voltage is increased upto a Certain limit. Hence it is called "Reverse Saturation Current"

The magnitude of Reverse Saturation Current depends on junction Temperature.

PN DIODE SYMBOL :



Fig.2. PN DIODE SYMBOL

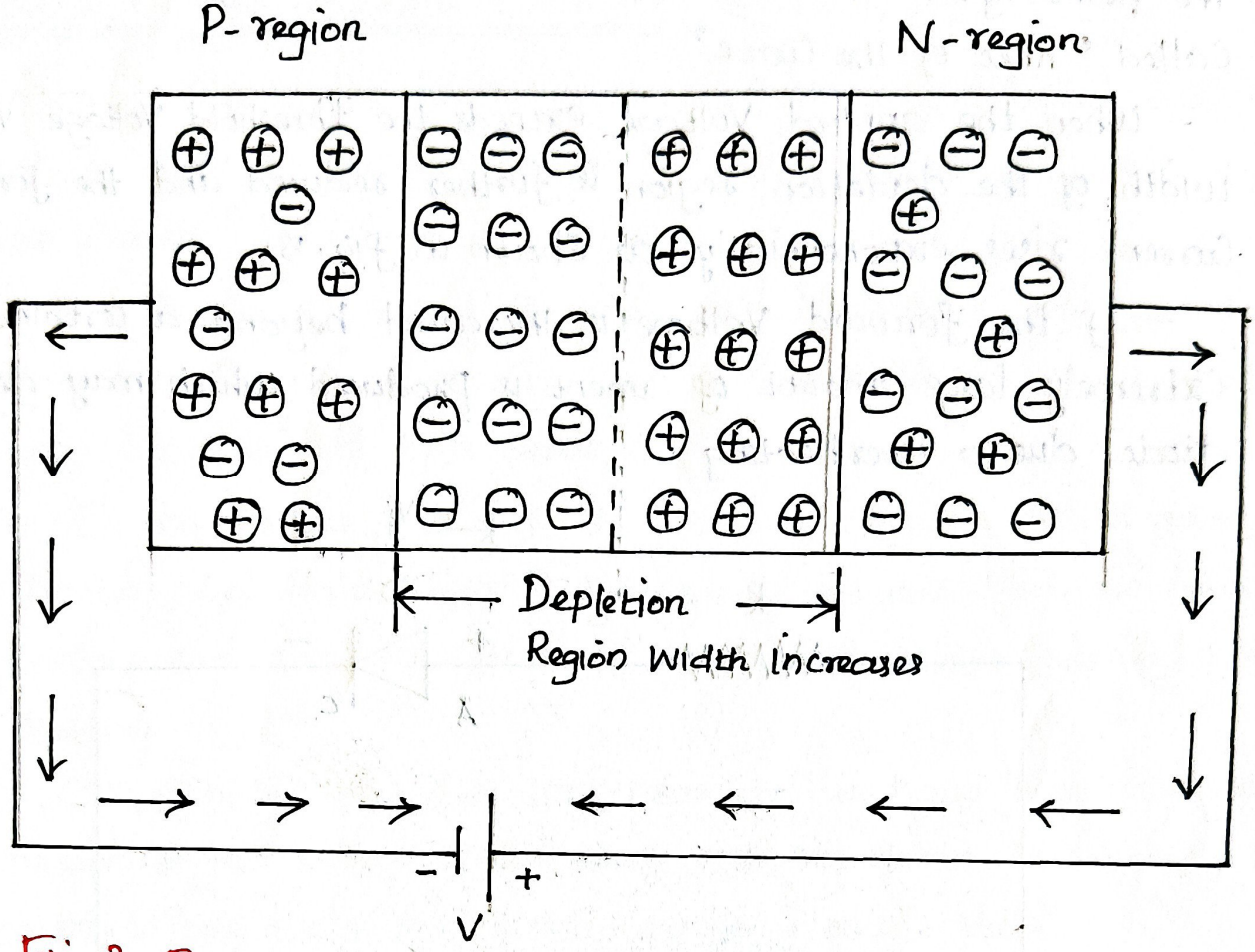


Fig. 3. Reverse Biased PN Junction

V-I CHARACTERISTICS OF PN DIODE

V-I characteristics is used for studying the response of P-N junction. Fig. 4 shows the circuit for V-I characteristics of P-N junction diode.

- It is defined as the graph of voltage applied across the P-N junction and the current flowing through the P-N junction. In fig. 5, the applied voltage is V and the voltage across the diode is 'V_f'.

FORWARD BIAS CHARACTERISTICS :

The current flowing in the circuit is the forward current 'I_f'. the graph of Forward Current I_f against the forward voltage 'V_f' across the diode is called 'forward characteristics of a diode'

As the voltage is applied, the current flow is very small upto the Cut in Voltage (V_c) or Knee Voltage (V_{Knee}) or Threshold voltage (V_{Th})

The point after which the current starts increasing exponentially is called 'Knee of the curve'

- When the applied voltage exceeds the threshold voltage V_{TH} the width of the depletion region is further reduced and the forward current rises exponentially as shown in fig. 5.

- If the forward voltage is increased beyond a certain value, extremely large amount of current is produced which may destroy the diode due to overheating.

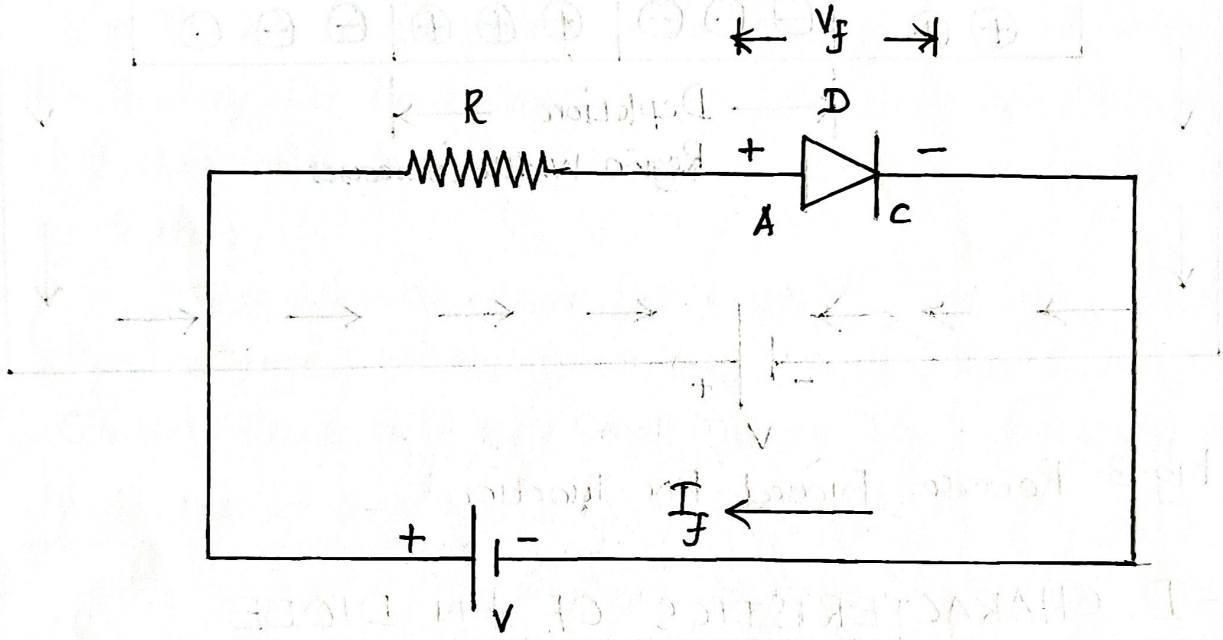


Fig. 4. Forward Biased PN diode.

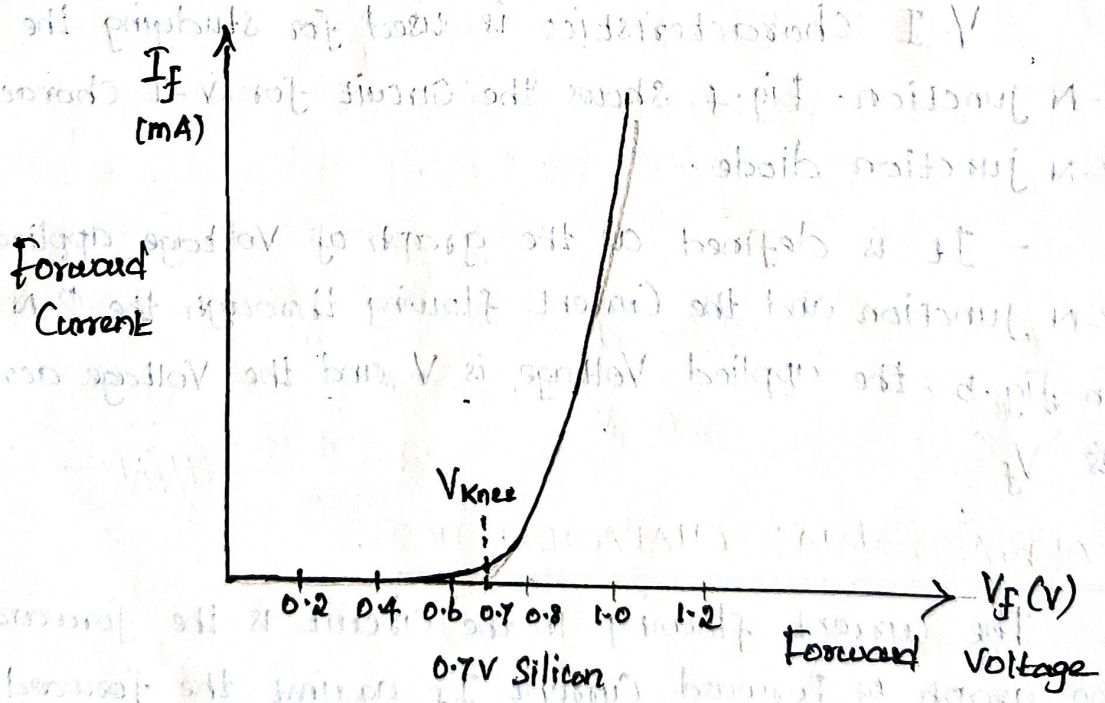


Fig. 5. Forward Biased PN diode characteristics.

REVERSE BIAS CHARACTERISTICS :

Fig·6 Shows the Reverse biased P-N diode. The Reverse Voltage across the diode is "V_R" and the current flowing through the diode is Reverse Current "I_R"

- The Reverse Current is mainly due to Minority Charge Carriers. The graph of Reverse Current 'I_R' Versus Reverse Voltage 'V_R' is Called Reverse characteristics of a diode.

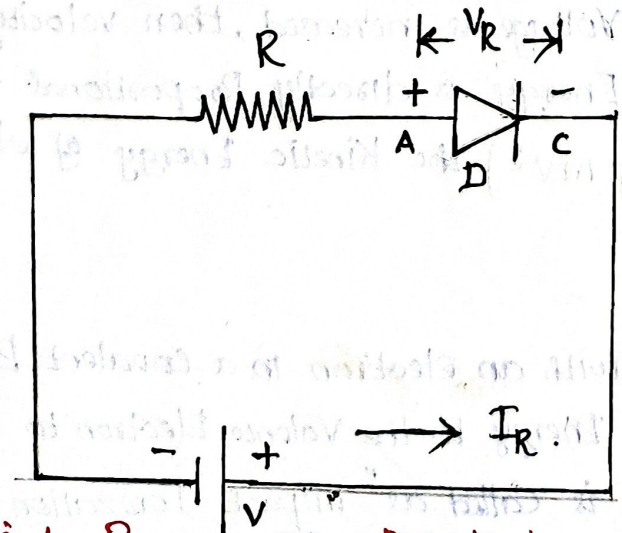
* During Reverse Bias, all the Majority Carriers are attracted by the Battery i.e, Holes from P-type move towards Negative terminal of battery and electrons from N-type move towards Positive terminal of Battery.

- Thus only Immobile ions near the junction form a strong depletion region which offers Very high resistance for Majority Carriers. Hence only very small Current flows in the Circuit

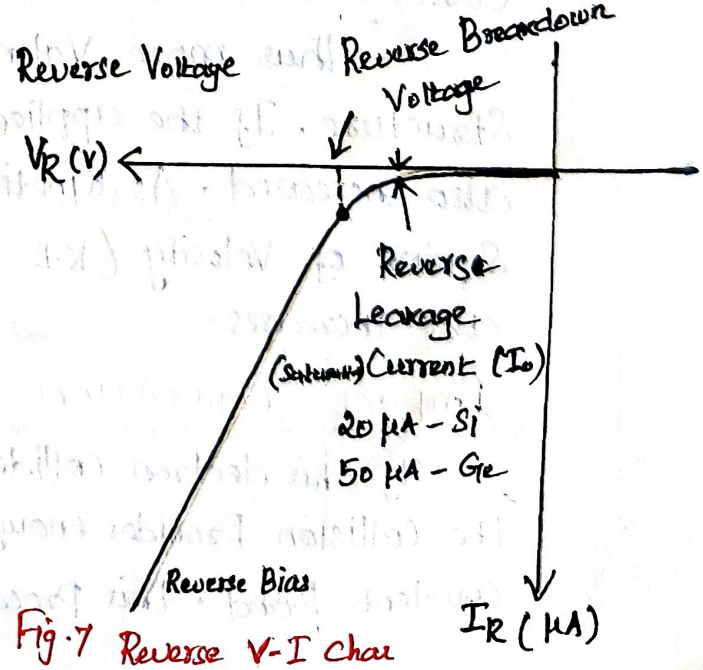
BREAKDOWN VOLTAGE (V_{BR})

A PN junction diode allows a very small amount of Current Called 'Reverse Saturation Current I_0', when it is reversebiased This Current is due to movement of Minority Carriers across the junction.

- If the applied reverse bias is increased to a Very large Value, large Current will flow through the diode which Causes damage to the junction. The Voltage at which this happens is known as the "Breakdown Voltage (V_{BR})".



Fig·6. Reverse Bias PN diode



Fig·7 Reverse V-I Char

BREAKDOWN IN PN DIODE

During Reverse Bias, when the Reverse Voltage is less than Breakdown Voltage, the diode Current is also very small due to Minority Carriers and almost Constant at I_0.

– When the Reverse Voltage is increased beyond the certain Limit, the diode Current will be maximum. The point at which the Current increases rapidly is called 'Breakdown' and the Corresponding Voltage is Called Reverse Breakdown Voltage 'V_{BR}'

* There are two types of Breakdown mechanisms in PN diode. They are

1. Avalanche Breakdown
2. Zener Breakdown.

1. AVALANCHE BREAKDOWN

The Reverse Bias causes a Small Reverse Current to flow in the device. This occurs due to the movement of Minority Charge Carriers, i.e., electrons from P-type and holes from N-type, Since Majority Carriers move away from the junction.

When the Reverse Bias is increased, the Minority Carriers acquire more Energy and this Kinetic Energy is Sufficient to break the Covalent Bonds of the Crystal Structure.

– Thus more Valence electrons are released from the Crystal Structure. If the applied Voltage is increased, then velocity is also increased. As Kinetic Energy is directly Proportional to Square of Velocity ($K.E = \frac{1}{2} mv^2$) the Kinetic Energy of electron also increases.

Impact Ionization :

If this electron collides with an electron in a Covalent Bond, then the Collision Provides enough Energy to the Valence Electron to Break its Covalent Bond. This Process is Called as 'Impact Ionization'

2. ZENER BREAKDOWN

Zener Breakdown occurs mainly in **Heavily doped diodes** where the **depletion Region** is Very small. When the diode is Reverse biased, the **electric field** across the depletion is Very Large

This very high electric field breaks the covalent bonds and pulls the electrons out of the Valence Bands. Hence, new 'electron-hole pairs' are created which Increases the Reverse Current and Large amount of Reverse Current across the junction. This Process is Called 'Zener Effect' This leads to breakdown in P-N diode is Called 'Zener Breakdown'.

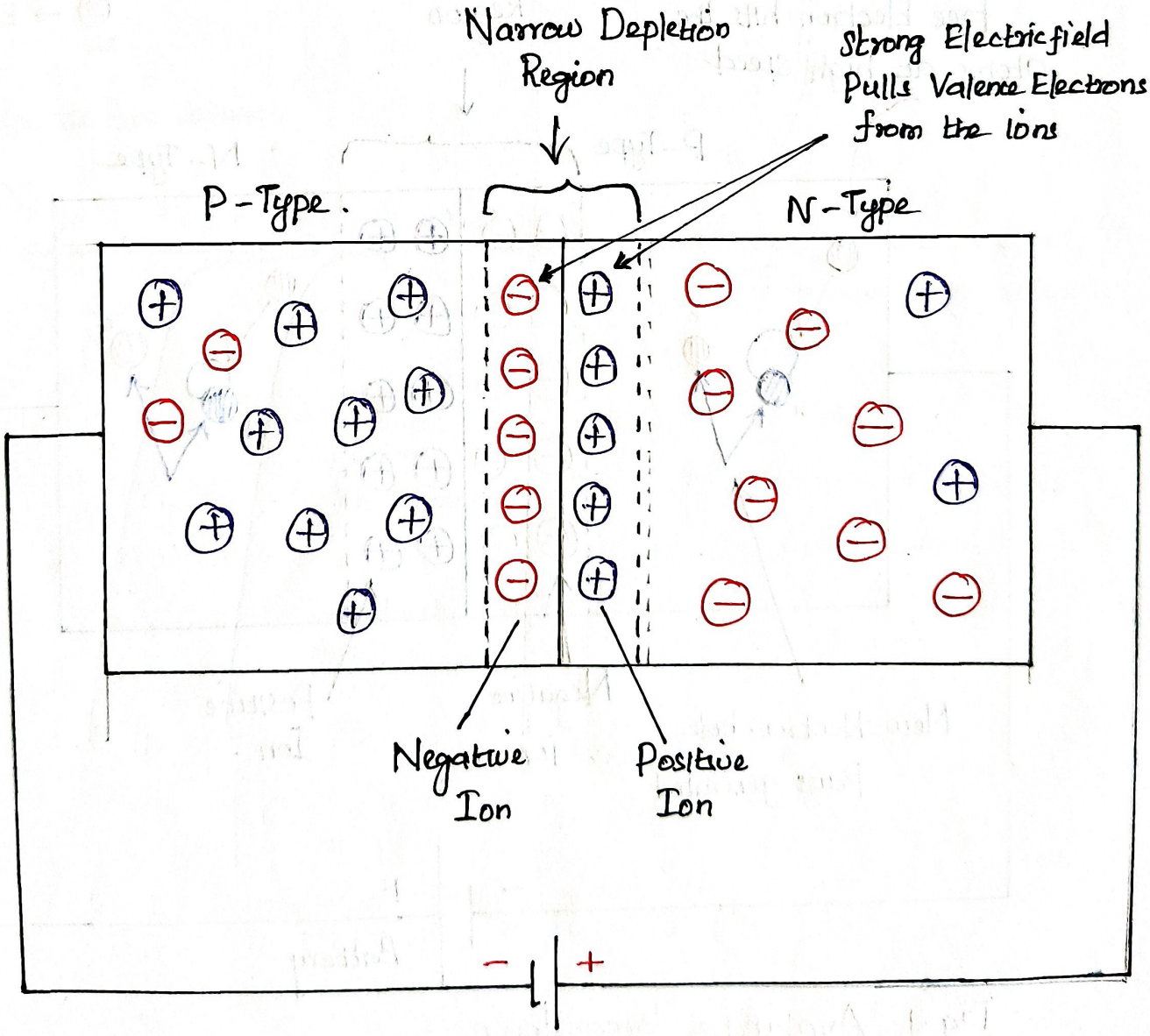


Fig. 2. Zener Breakdown

Hence, 'electron-hole pairs' are created. These electron-hole pairs in turn participate in collision and generate 'New Electron-hole pairs' This process is called as Avalanche Multiplication or Carrier Multiplication.

* It is a Cumulative Process and Large Number of Electron-hole pairs are created. The Reverse Current Increases rapidly and the junction is said to be in 'Breakdown Region'

The 'avalanche Breakdown' occurs only in lightly doped diodes, where the depletion region is very wide and the electric field is very Low.

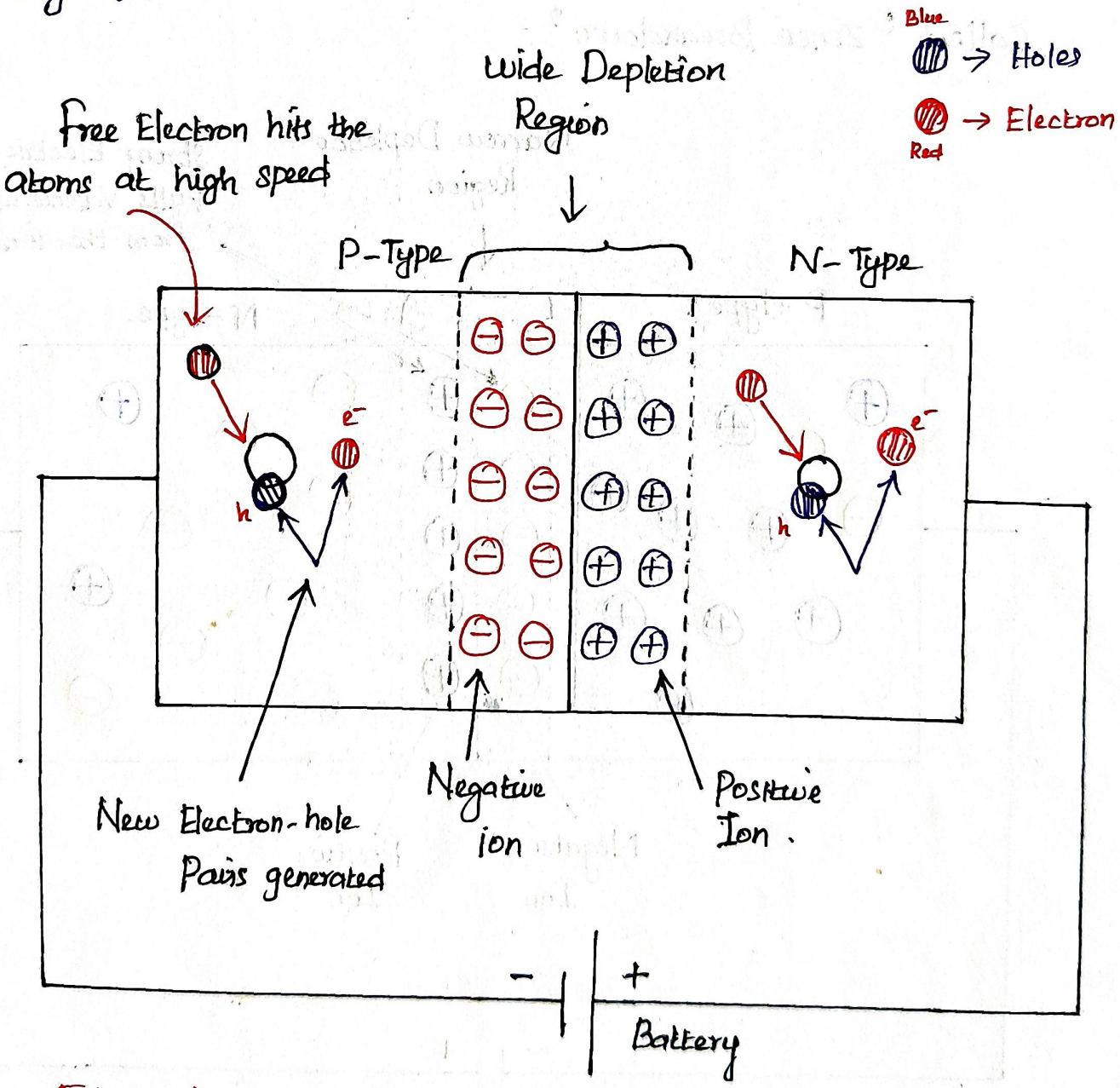


Fig.1 Avalanche Breakdown

For diodes with Reverse Breakdown between 5V & 6V, both avalanche and Zener Mechanisms occurs if the Breakdown Voltage is less than 5V ($V_{Br} < 5V$) then "Zener Breakdown" occurs.

- The Breakdown Voltage depends upon the doping Level of the Junction. This Value determines the practical Safe operating Voltage called Peak Inverse Voltage (PIV) of a diode. If the operating voltage is less than PIV Rating ($V <$ PIV rating), the Reverse Breakdown Condition is Prevented.

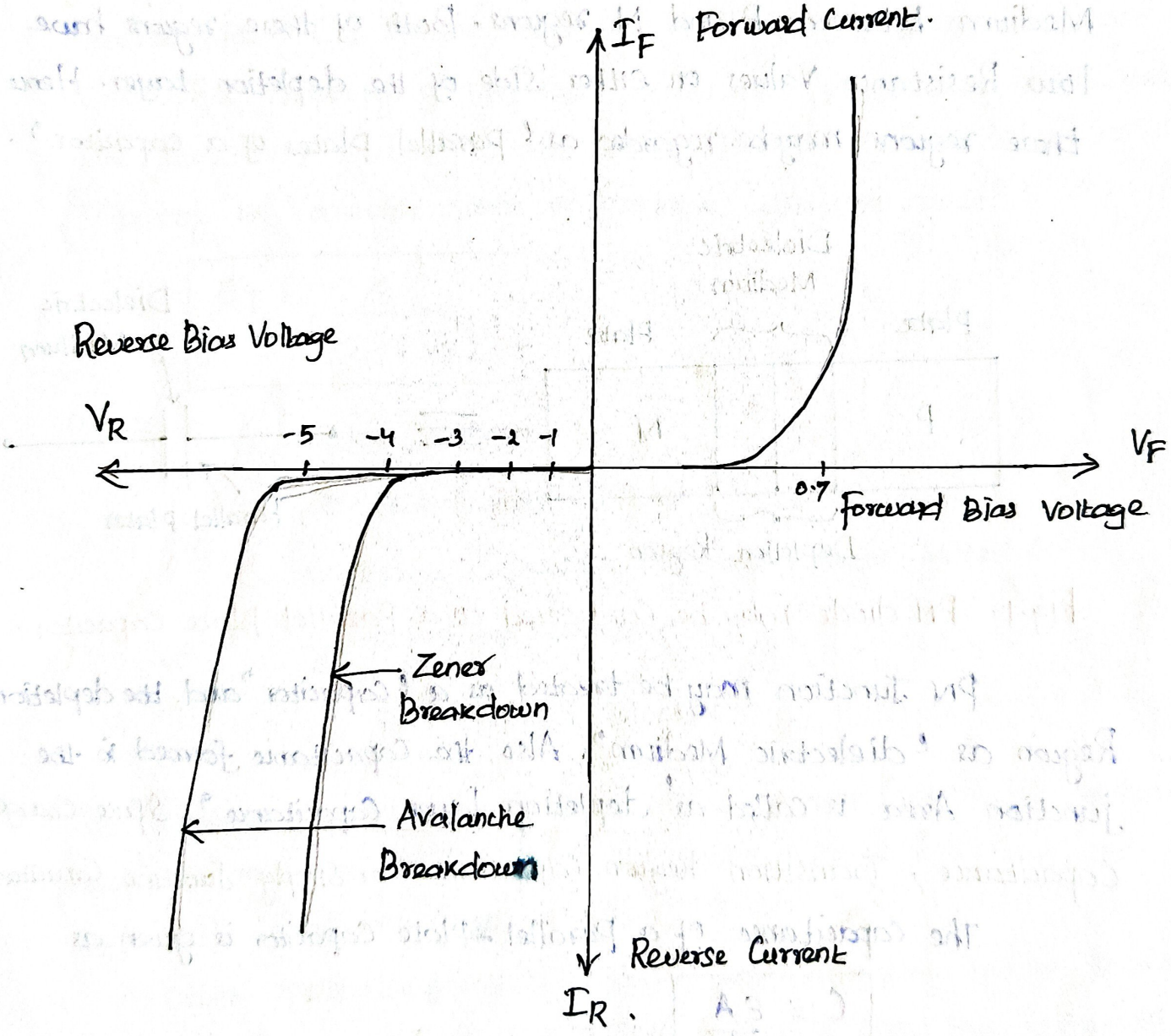


Fig. 3 Breakdown characteristics.

TRANSITION AND DIFFUSION CAPACITANCES

1. PN DIODE AS PARALLEL PLATE CAPACITOR

Capacitive Effects are exhibited by PN junctions when they are either forward-biased or Reverse Biased

- We know that, the width of the depletion Layer decreases when the PN junction is forward biased. Similarly, the width of the depletion layer increases, when the junction is Reverse biased.

* Here the depletion Layer acts as a dielectric or Non-conductive Medium between P and N regions. Both of these regions have low Resistance Values on either side of the depletion Layer. Hence those regions may be regarded as 'parallel plates of a capacitor'.

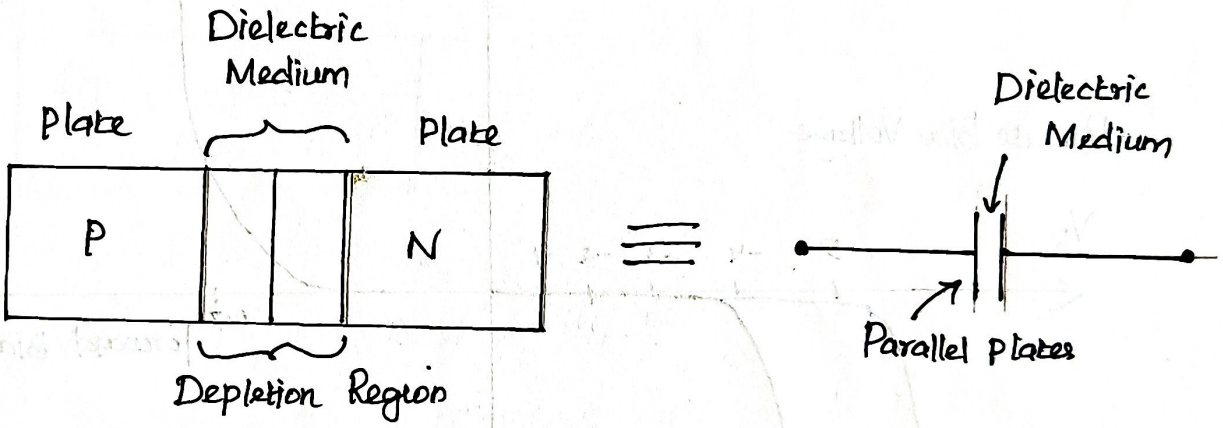


Fig.1. PN diode may be considered as a Parallel Plate capacitor.

PN Junction may be treated as a 'capacitor' and the depletion Region as 'dielectric Medium'. Also the Capacitance formed in the junction Area is called as 'depletion layer Capacitance', Space Charge Capacitance, Transition Region Capacitance or Simply Junction Capacitance.

The Capacitance of a Parallel-Plate Capacitor is given as

$$C = \frac{\varepsilon A}{d}$$

where

ε - Permittivity of the dielectric (Insulator between the plates

of Area 'A' separated by a distance 'd'

Its typical Value is 40 PF.

Two types of Capacitances Such as Transition and Diffusion as below:

2. TRANSITION CAPACITANCE OR SPACE-CHARGE CAPACITANCE (C_T)

When a PN Junction is Reverse biased, the depletion Region acts like an 'Insulator' or as a 'dielectric'

* The P and N regions on either sides have Low Resistance and act as the plates. Hence it is similar to a 'Parallel Plate Capacitor'. This junction Capacitance is called Transition or Space charge Capacitance (C_T)

Since the thickness of the depletion Layer depends on the amount of Reverse Bias, C_T can be Controlled with the help of applied Bias.

- This property of Variable Capacitance (Possessed by a Reversebiased PN Junction) is used in the Construction of a device known as 'Varicap or Varactor diode or Variable Capacitor diode'

$$C_T = \frac{K}{(V_K + V_R)^n}$$

where V_K - Knee Voltage

V_R - Applied Reverse Voltage

k - Constant depending on semiconductor Material.

$n = \frac{1}{2}$ for alloy Junction

$= \frac{1}{3}$ for diffused Junction.

The Voltage-Variance Capacitance of a Reverse Biased PN Junction is used in many circuits. One such application is in an FM Tuner as Automatic Frequency Control (AFC)

- Other applications are: used in Self-balancing Bridge circuits, Electronic Tuners in TV and in special type of Amplifiers known as Parametric Amplifiers.

3. DIFFUSION OR STORAGE CAPACITANCE (C_D)

This capacitive Effect is Present when the Junction is forward-biased It is called as 'diffusion Capacitance' C_D, due to the time delay in

Minority charges across the junction by diffusion Process. Hence, this Capacitance cannot be identified interms of a 'dielectric and plates'

* It Varies directly with forward current. When the forward biased PN junction is Suddenly Reverse biased, a Reverse current flows which is large initially, but gradually decreases to the Level of Saturation Current 'I₀'

This effect can be likened to the discharging of a capacitor. therefore it is called 'diffusion Capacitance C_D' Its typical Value is 0.02 μF.

* This Capacitance plays an important role in the operation of the devices which are required to Switch rapidly from Forward Bias to Reverse Bias. This Switch over Cannot be quick, if C_D is large. i.ey it will delay both the Switch-ON and Switch-OFF. This effect of C_D is referred to as 'Recovery-Time or Carrier Storage'

It is given by

$$C_D = \frac{dQ}{dV}$$

$$C_D = \frac{\tau I_0}{\eta V_T} e^{V/\eta V_T} \approx \frac{\tau I}{\eta V_T}.$$

$$\boxed{C_D = \frac{\tau I}{\eta V_T}}$$

Where,

τ = Mean life time of charge carriers

η = Constant = 2 for Si and 1 for Ge

I = Forward current

I_0 = Reverse Saturation current

V_T = Volt Equivalent of Temperature.

RECTIFIER

A rectifier is an electrical device that converts alternating Current (AC) (which periodically reverse direction) to direct Current (dc) which flows in only one direction. This Process is called 'rectification'

APPLICATION : Rectifiers are used in power supplies for Radio, Television and Computer Equipment.

PN DIODE :

A PN diode is a two terminal device which conducts and Current flows through it without any Resistance during 'forward bias Condition' when the diode is 'Reverse Biased' the diode will not Conduct due to high Resistance and No Current flows through the diode i.e, diode is in OFF Condition.

IDEAL DIODE :

The Ideal diode acts as a switch either ON or OFF depending on the Voltage applied to the diode. Since Ideal diode has Zero Resistance under 'forward Bias' and infinite Resistance under 'Reverse Bias'

HALF WAVE RECTIFIER

In Half-wave Rectifier, either positive or Negative half of the ac Signal is passed, while other half is blocked.



- It Converts an AC Voltage into a DC Voltage during one half of the AC cycle only.

* PN diode is used for Rectification because of its Unidirectional Property i.e, Conducts during Forward Bias and doesnot Conduct during Reverse Bias.

Fig. 1 Shows the Circuit diagram of Half wave Rectifier.

Let V_i be the input Voltage to the Primary of the Transformer, and is given as

$$V_i = V_m \sin \omega t, \quad V_m >> V_\gamma$$

Where, V_γ - Cut in Voltage of the diode.

1 During Positive Half Cycle of the input Signal, the diode is forward biased and the anode of the diode is more positive with respect to Cathode. The diode therefore Conducts during positive Cycle of the Input Voltage.

During Negative Half Cycle of the input signal, the diode is Reverse biased and the Anode of the diode is Negative with respect to Cathode. Thus the diode D does not Conduct due to high Impedance. Hence the Input Voltage does not appear at the output

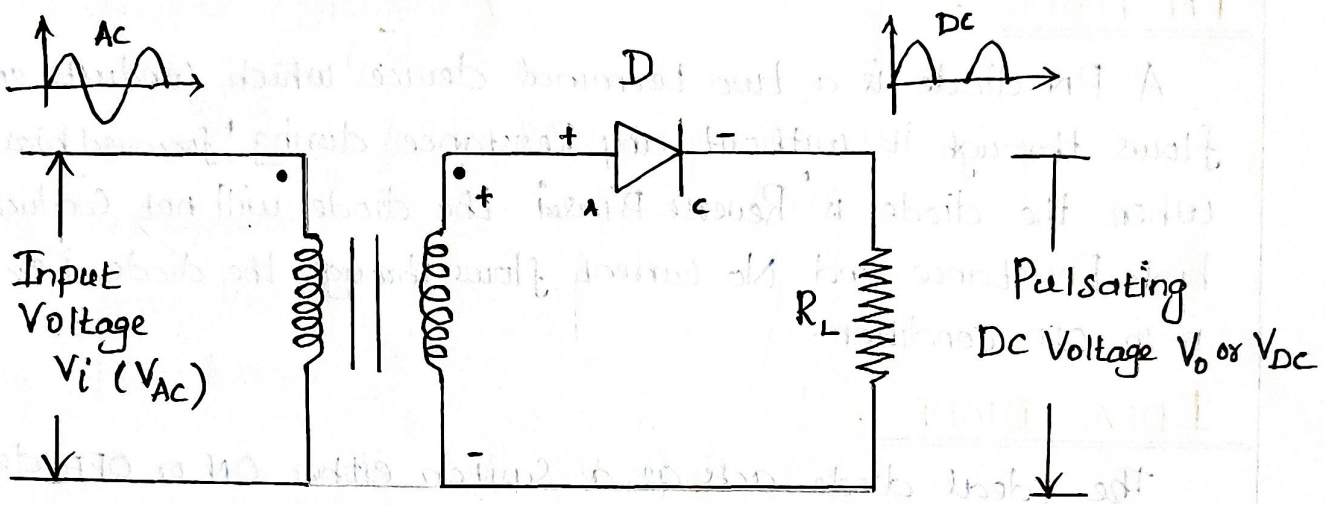


Fig.1 Half-Wave Rectifier.

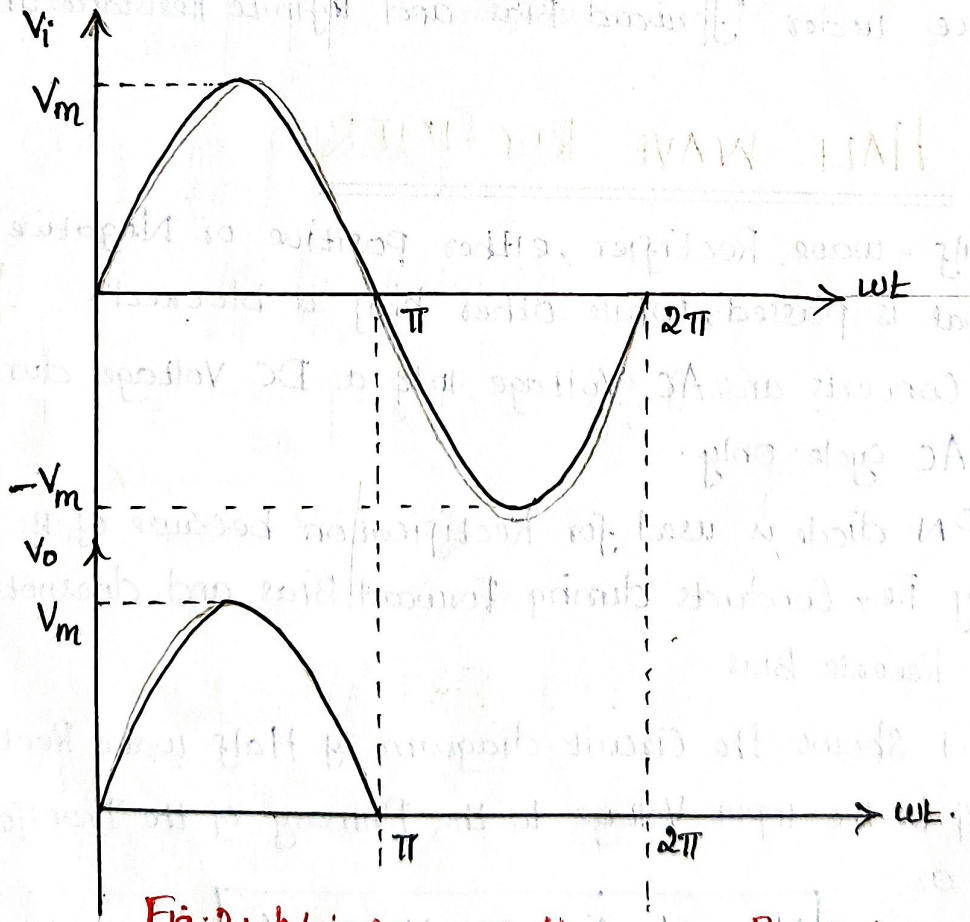


Fig.2. Waveform of Half-wave Rectifier.

Fig.2 Shows the input and Output waveform of Half wave Rectifier.

ANALYSIS :

In the analysis of a HWR, the following Parameters to be analyzed

1. Average Voltage (dc output Voltage) V_{av}
2. Average Current (DC output Current) I_{av}
3. RMS Voltage (AC Input Voltage) V_{rms}
4. RMS Current (AC Input Current) I_{rms}
5. Rectifier Efficiency (η)
6. Ripple Factor (γ)
7. Peak Inverse Voltage (PIV)
8. Transformer Utilization Factor (TUF)
9. Form Factor
10. Peak Factor

1. AVERAGE VOLTAGE ($V_{av} = V_{dc}$) : ✓

$$V_{dc} = \frac{1}{2\pi}\left[\int_0^{\pi} V_m \sin\omega t \, d(\omega t) + \int_{\pi}^{2\pi} 0 \cdot d(\omega t)\right]$$

$$= \frac{V_m}{2\pi}\left[-\cos\omega t\right]_0^{\pi} + 0$$

$\cos\pi = -1$

$\cos 0 = 1$

$$= \frac{-V_m}{2\pi}\left[\cos\pi - \cos 0\right]$$

$$= \frac{-V_m}{2\pi}\left[-1-1\right] = \frac{-V_m}{2\pi}(-2)$$

$$\boxed{V_{dc} = V_{av} = \frac{V_m}{\pi}}$$

2. AVERAGE CURRENT ($I_{av} = I_{dc}$) :

$$I_{dc} = \frac{V_{dc}}{R_L}$$

$$\boxed{I_{dc} = \frac{V_m}{\pi R_L}}$$

3. RMS VOLTAGE (V_{rms})

$$V_{rms}^2 = \frac{1}{2\pi}\int_0^{\pi} V_i^2 \, d(\omega t) \qquad (V_i = V_m \sin\omega t)$$

$$\sin^2\omega t = \frac{1-\cos 2\omega t}{2}$$

$$= \frac{1}{2\pi}\int_0^{\pi} V_m^2 \sin^2\omega t \, d(\omega t)$$

$$= \frac{V_m^2}{2\pi}\int_0^{\pi} \frac{1-\cos 2\omega t}{2} \, d(\omega t)$$

$$= \frac{V_m^2}{4\pi}\left[\int_0^{\pi} d(\omega t) - \int_0^{\pi} \cos 2\omega t \, d(\omega t)\right]$$

$$= \frac{V_m^2}{4\pi}\left[\pi - \left(\frac{\sin 2\omega t}{2}\right)_0^{\pi}\right] \qquad \therefore \sin 2\theta = 0$$

$$V_{rms}^2 = \frac{V_m^2}{4\pi}(\pi - 0) = \frac{V_m^2}{4}$$

$$\boxed{V_{rms} = \frac{V_m}{2}}$$

4. RMS CURRENT (I_{rms})

$$I_{rms} = \frac{V_{rms}}{R_L}$$

$$\boxed{I_{rms} = \frac{V_m}{2R_L}}$$

5. RECTIFIER EFFICIENCY : (η)

The efficiency η is defined as the ratio of dc output power to Ac input power.

$$\eta = \frac{\text{dc Output Power}}{\text{ac Input Power}} = \frac{P_{dc}}{P_{ac}} = \frac{\frac{(V_{dc})^2}{R_L}}{\frac{V_{rms}^2}{R_L}} = \frac{\left(\frac{V_m}{\pi}\right)^2}{\left(\frac{V_m}{2}\right)^2}$$

$$\eta = \frac{V_m^2}{\pi^2} \times \frac{2^2}{V_m^2} = \frac{4}{\pi^2} = 0.406.$$

$$\eta = 0.406 = 40.6\ \%$$

The Maximum Efficiency of a half-wave Rectifier is 40.6 %.

6. RIPPLE FACTOR (γ)

$$\gamma = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{V_m/2}{V_m/\pi}\right)^2 - 1} = \sqrt{\left(\frac{V_m^2/4}{V_m^2/\pi^2}\right) - 1} = \sqrt{\left(\frac{V_m^2}{4} \times \frac{\pi^2}{V_m^2}\right) - 1}$$

$$= \sqrt{\frac{\pi^2}{4} - 1}$$

$$\gamma = 1.21$$

7. PEAK INVERSE VOLTAGE (PIV)

Peak Inverse Voltage (PIV) is defined as the maximum reverse Voltage a diode can withstand destroying the junction

$\boxed{PIV = V_m}$ i.e., Peak of the Negative Half cycle.

8. TRANSFORMER UTILIZATION FACTOR (TUF)

This indicates the Rating of the transformer. This can be found by the ratio of dc Power delivered to the load to the ac rating of the Transformer.

$$TUF = \frac{P_{dc}}{P_{ac}\ (rated)} = \frac{\left(\frac{I_m}{\pi}\right)^2 R_L}{\frac{V_m}{\sqrt{2}} \cdot \frac{I_m}{2}} = \frac{2\sqrt{2}}{\pi^2} = 0.287$$

9. FORM FACTOR

It is defined as the Ratio of RMS Value to the Average

$$\text{Form Factor} = \frac{\text{RMS Value}}{\text{Average Value}} = \frac{V_m/2}{V_m/\pi} = \frac{\pi}{2} = 1.57$$

10. PEAK FACTOR :

Peak factor is defined as the Ratio of Peak Value to the RMS value

$$\text{Peak Factor} = \frac{\text{Peak Value}}{\text{RMS Value}} = \frac{V_m}{V_m/2} = 2.$$

FULL WAVE RECTIFIER

Full wave Rectifier Converts an AC Voltage into pulsating DC Voltage during both half cycles of the applied Voltage.

Full wave Rectifiers are classified into

1. Centre-tapped Full wave Rectifier.
2. Full wave Bridge Rectifier

1. CENTRE-TAPPED FULL WAVE RECTIFIER :

A Centre tapped full wave Rectifier Consists of

i) Centre-tapped transformer

ii) Two Diodes

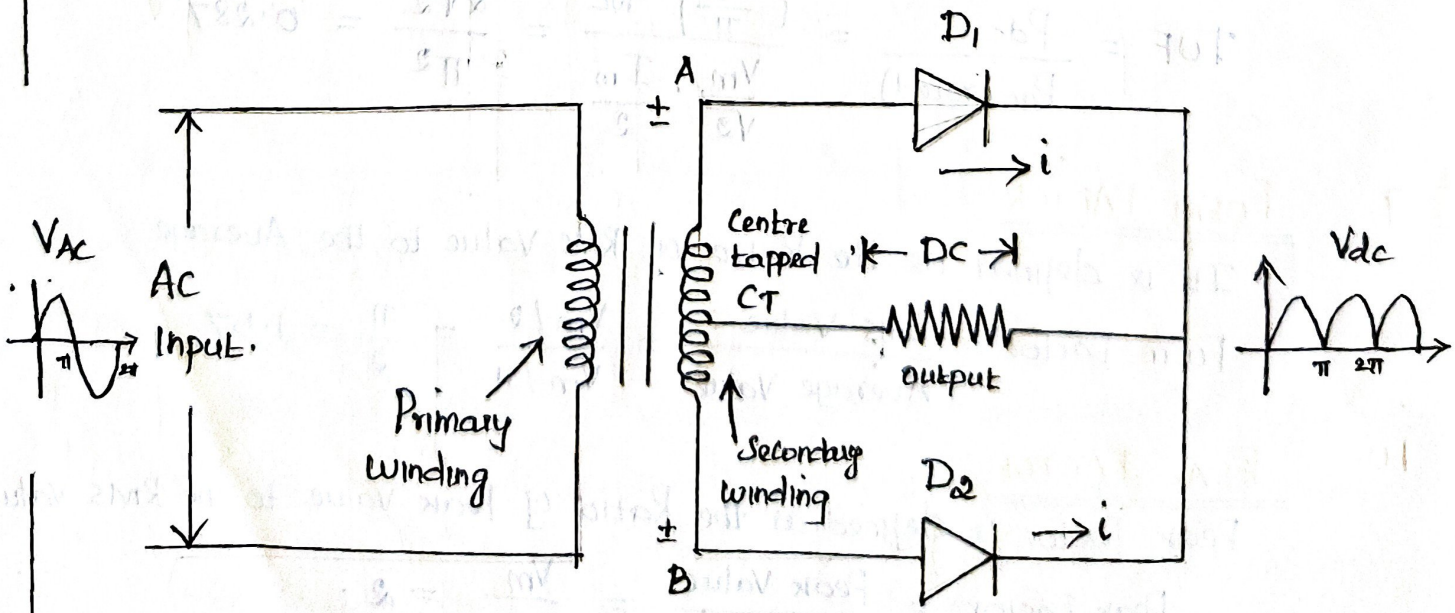
iii) Resistive Load.

CENTRE-TAPPED TRANSFORMER :

It is a normal Transformer with one slight modification. It has an additional wire connected to the exact Centre of the Secondary winding

- This type of Construction divides the AC voltage into two equal and opposite Voltages, namely positive Voltage (V_a) and Negative Voltage (V_b)

The total output voltage $\boxed{V = V_a + V_b}$



During the positive half cycle of the Ac voltage, terminal A will be positive, centre-tap will be at zero potential, and terminal B will be Negative potential.

This will lead to forward bias diode D_1 and cause current to flow through it. During this time, diode D_2 is in Reverse Bias and will block current through it.

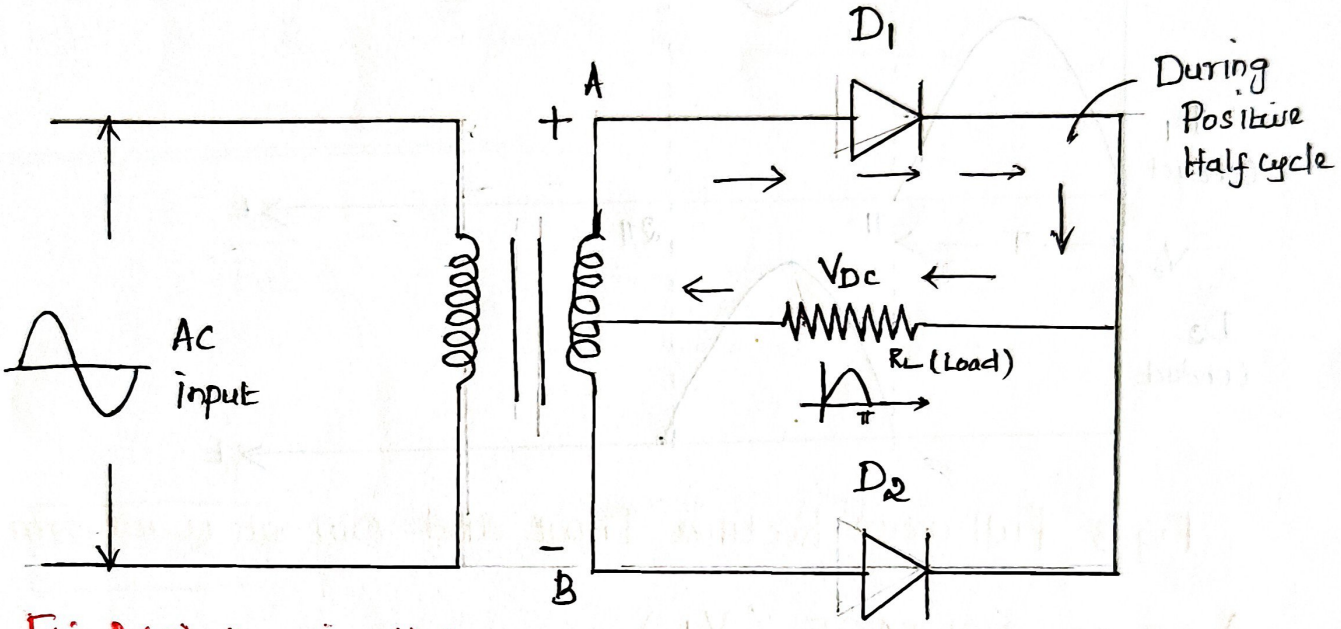


Fig. 2(a) Positive Half cycle

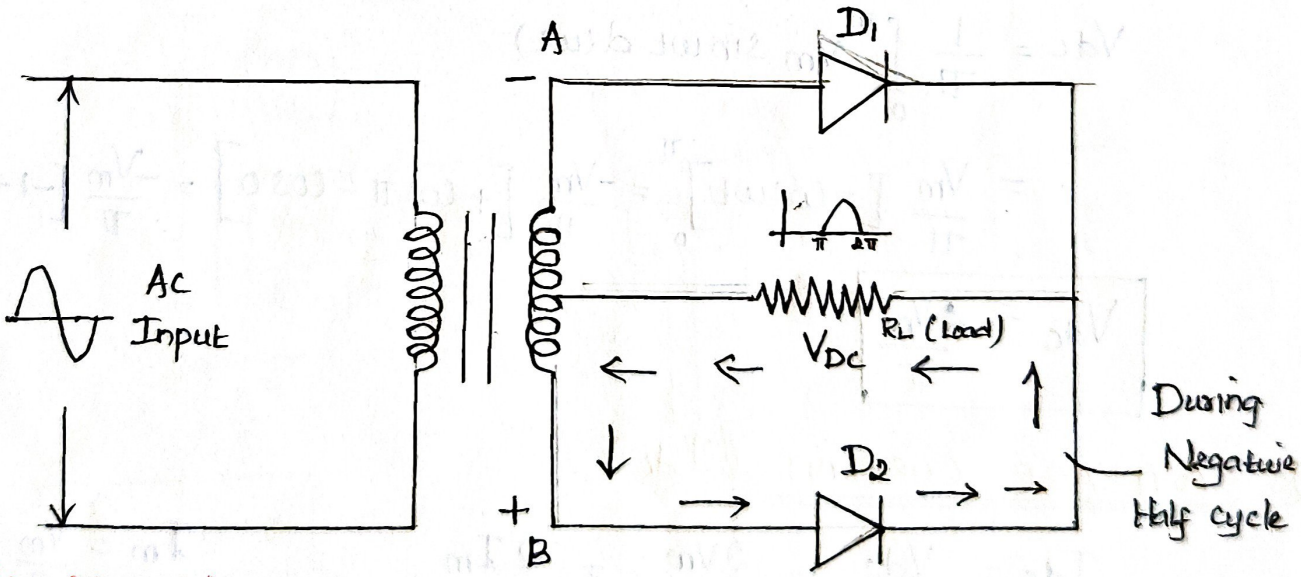


Fig. 2(b) Negative Half cycle.

During the Negative Half cycle of the Ac voltage, terminal 'B' will be positive and terminal 'A' will be Negative and centre-tap will be zero.

- This will lead to forwarding Bias in diode D_2 and cause current to flow through it. During this time, diode D_1 is in Reverse Bias and will block current through it.

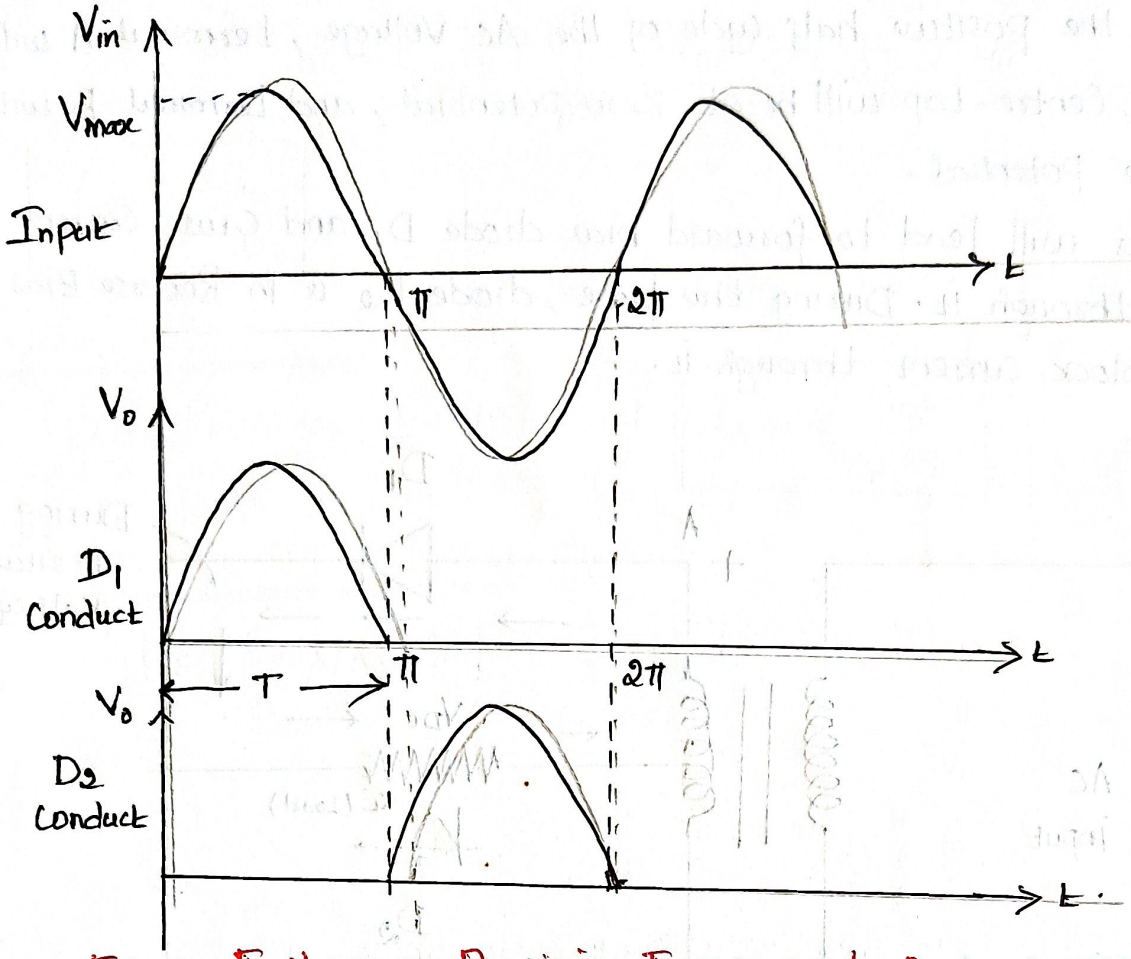


Fig.3 Full wave Rectifier Input and Output waveform.

1. AVERAGE VOLTAGE (V_{dc})

$$V_{dc} = \frac{1}{\pi}\int_0^{\pi} V_m \sin\omega t \, d(\omega t)$$

$$= \frac{V_m}{\pi}\left[-\cos\omega t\right]_0^{\pi} = \frac{-V_m}{\pi}\left[+\cos\pi - \cos 0\right] = \frac{-V_m}{\pi}\left[-1-1\right]$$

$$\boxed{V_{dc} = \frac{2V_m}{\pi}}$$

2. AVERAGE CURRENT (I_{dc}):

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{2V_m}{\pi R_L} = \frac{2I_m}{\pi} \qquad I_m = \frac{V_m}{R_L}$$

$$\boxed{I_{dc} = \frac{2I_m}{\pi}}$$

3. RMS VALUE OF VOLTAGE (V_{RMS})

$$V_{rms}^2 = \frac{1}{\pi}\int_0^{\pi} V_m^2 \sin^2\omega t \, d(\omega t) = \frac{V_m^2}{\pi}\int_0^{\pi} \frac{1-\cos 2\omega t}{2} d(\omega t).$$

$$= \frac{V_m^2}{2\pi}\left[\omega t - \frac{\sin 2\omega t}{2}\right]_0^{\pi} = \frac{V_m^2}{2\pi}[\pi - 0] = \frac{V_m^2}{2}$$

$$\boxed{V_{rms} = \frac{V_m}{\sqrt{2}}}$$

4. RMS CURRENT (I_{RMS})

$$I_{rms} = \frac{V_{rms}}{R_L} = \frac{V_m}{\sqrt{2}R_L} \quad \therefore \quad \boxed{I_{rms} = \frac{V_m}{\sqrt{2}R_L}}$$

5. RECTIFIER EFFICIENCY (η) :

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{\frac{V_{dc}^2}{R_L}}{\frac{V_{rms}^2}{R_L}} = \frac{\left(\frac{2V_m}{\pi}\right)^2}{\left(\frac{V_m}{\sqrt{2}}\right)^2} = \frac{\frac{4V_m^2}{\pi^2}}{\frac{V_m^2}{2}} = \frac{4V_m^2}{\pi^2} \times \frac{2}{V_m^2}$$

$$\eta = \frac{8}{\pi^2} = 0.812$$

$\boxed{\eta = 81.2\%}$ Maximum Efficiency of FWR is 81.2%.

6. RIPPLE FACTOR (γ)

$$\gamma = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{(V_m/\sqrt{2})}{2V_m/\pi}\right)^2 - 1} = \sqrt{\frac{V_m^2/2}{4V_m^2/\pi} - 1} = \sqrt{\frac{V_m^2}{2} \times \frac{\pi}{4V_m^2} - 1}$$

$$= \sqrt{\frac{\pi^2}{8} - 1}$$

$$\boxed{\gamma = 0.482}$$

7. TRANSFORMER UTILIZATION FACTOR (TUF)

The average TUF of Full wave Rectifier is 0.693.

8. FORM FACTOR :

$$\text{Form factor} = \frac{\text{RMS Value}}{\text{Average Value}} = \frac{V_m/\sqrt{2}}{2V_m/\pi} = \frac{V_m}{\sqrt{2}} \times \frac{\pi}{2V_m} = \frac{\pi}{2\sqrt{2}} = 1.11.$$

9. **PEAK FACTOR :**

$$\text{Peak Factor} = \frac{\text{Peak Value of the Output Voltage}}{\text{RMS Value of the Output Voltage}}.$$

$$= \frac{V_m}{V_m/\sqrt{2}} = \frac{V_m}{V_m}\sqrt{2} = \sqrt{2}. \quad \therefore \boxed{PF = \sqrt{2}}$$

10. **PEAK INVERSE VOLTAGE (PIV)**

The PIV for Full wave Rectifier is $2V_m$ $\therefore \boxed{PIV = 2V_m}$

FULL WAVE BRIDGE RECTIFIER

The Centre tapping is eliminated in the bridge Rectifier. In this rectifier, four diodes are connected to form a 'bridge'

- The Ac Input Voltage is applied to the diagonally opposite ends of the bridge. The other two ends of the bridge are connected to the Load Resistance. Fig.1 shows the bridge Rectifier using four diodes.

*

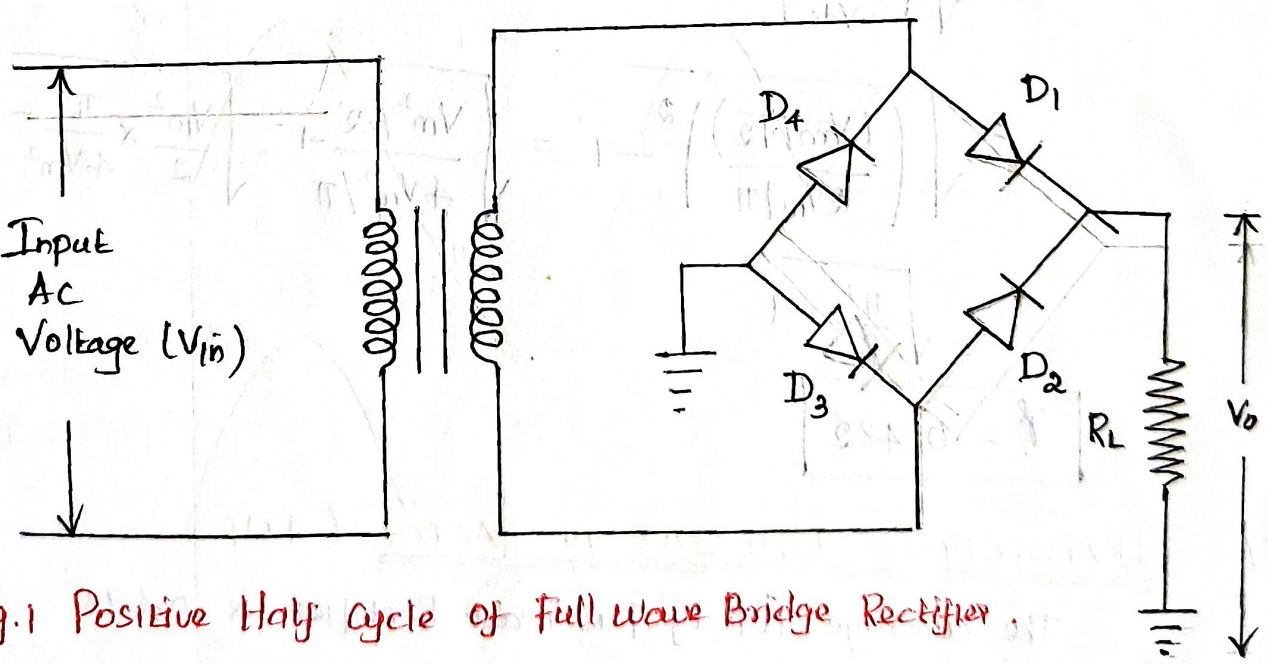


Fig.1 Positive Half cycle of Full wave Bridge Rectifier.

During Positive Half cycle of the Input Voltage, diode D_1 and D_3 Conduct and diode D_2 and D_4 do not Conduct.

- The Current is Produced due to diode D_1 and D_3 and this Current flows through the Load Resistance R_L

During Negative Half cycle of the input ac voltage, diodes D_2 and D_4 Conduct and Diodes D_1 and D_3 do not conduct. The Current flows in the Load Resistance R_L due to diodes D_2 and D_4.

- The Current flows in the same direction in both Positive and Negative Half cycles of the input voltage, thus an Unidirectional output waveform is obtained.

* The Maximum Efficiency of a Bridge Rectifier is 81.2% and the Ripple factor is 0.48, PIV is V_m. fig.3 shows Output waveform of FWR

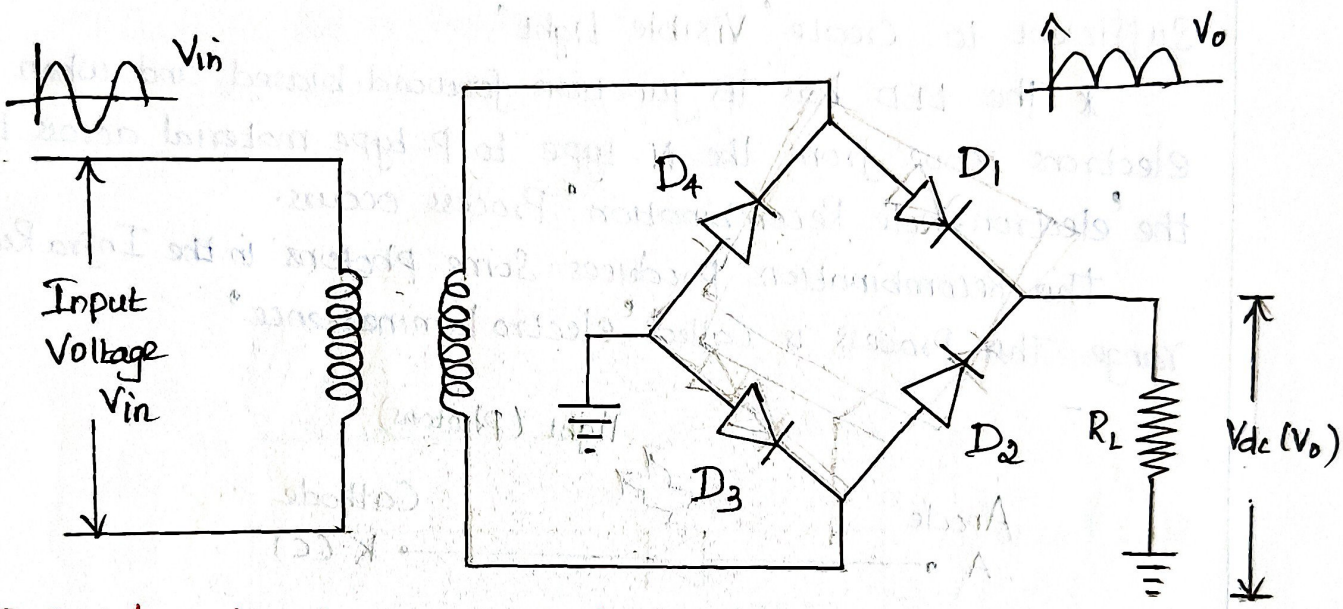


Fig.2 Negative Half cycle of FW BRIDGE RECTIFIER.

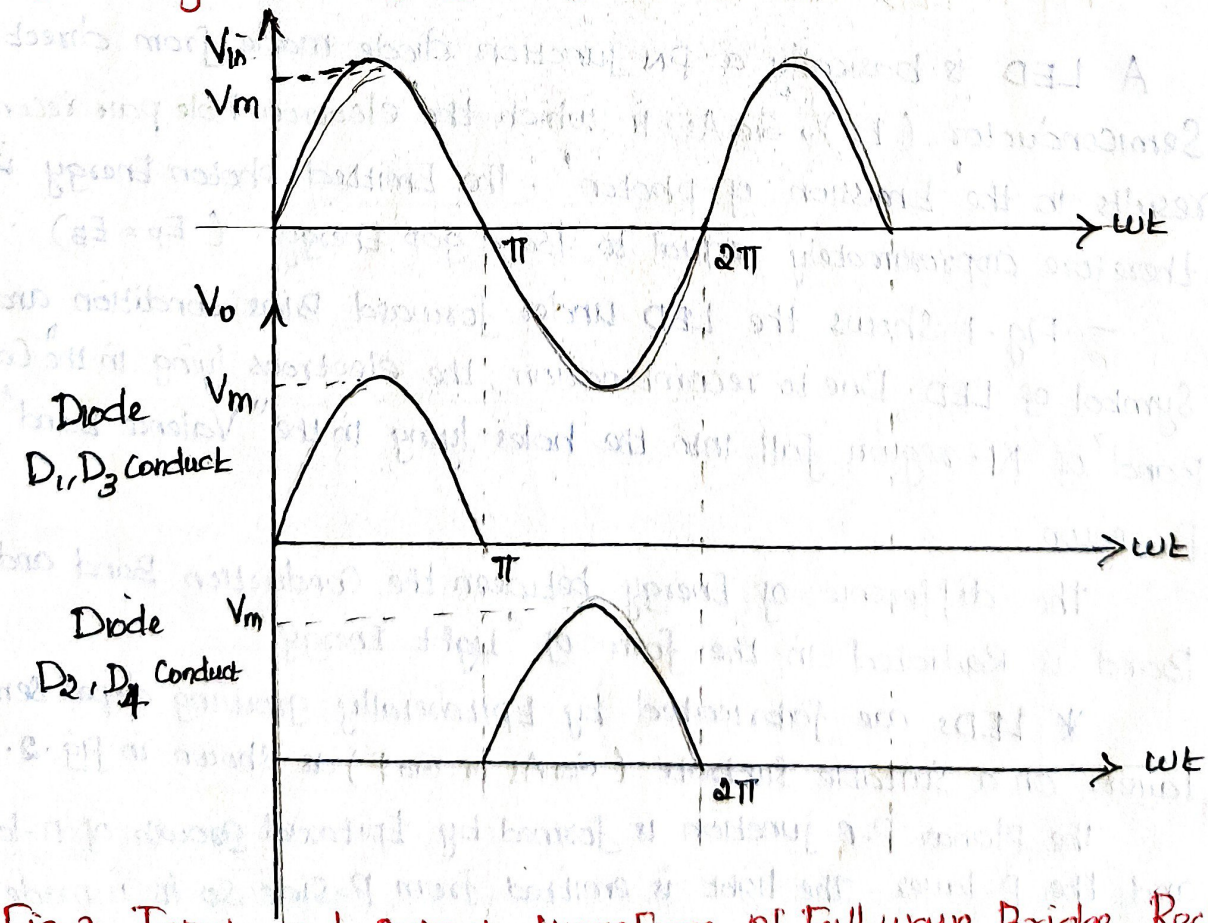


Fig.3. Input and Output Waveform of Full wave Bridge Rectifier.

LIGHT EMITTING DIODES (LED)

LEDs are PN junction devices Constructed from Gallium Arsenide (GaAs), Gallium Arsenide phosphide (GaAsP) or Gallium Phosphide (GaP).

- Silicon (Si) and Germanium (Ge) are not suitable because the junctions produce heat and IR or Visible light cannot be Produced. In GaP or GaAsP, the number of photons of light energy is Sufficient to Create 'Visible Light'

* The LED has its junction forward biased and when the electrons move from the N-type to P-type material across the junction, the 'electron-hole Recombination' Process occurs.

This Recombination produces Some photons in the Infra Red (IR) range. This Process is Called 'electro luminescence'

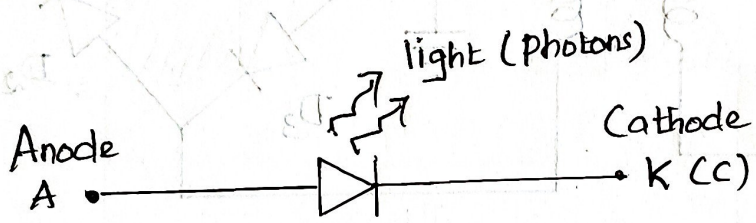


Fig.1. LED and its Symbol.

A LED is basically a PN junction diode made from direct Bandgap Semiconductor (Ex), GaAs in which the 'electron-hole pair recombination' results in the 'Emission of photon'. The Emitted photon Energy is therefore approximately equal to Band gap Energy ($E_p = E_B$).

- Fig.1 Shows the LED under forward Bias Condition and the Symbol of LED. Due to recombination, the electrons lying in the 'Conduction Band" of N-region fall into the holes lying in the "Valence band" of P-region

The difference of Energy between the Conduction Band and Valence Band is Radiated in the form of 'Light Energy'

* LEDs are fabricated by Epitaxially growing doped Semiconductor layers on a Suitable Substrate (GaAs or GaP) as shown in fig.2.

The planar P-n junction is formed by Epitaxial growth of n-layer and the P-layer. The light is emitted from P-Side so it is made Narrow to allow the photons to escape.

N-Side is heavily doped so that most recombination take place in P-side. The Efficiency of generation of light increase with increase in injected current and with decrease in temperature.

* LEDs radiate different colours such as Red, Green, Yellow, Orange, Blue and White. The wavelength of light emitted depends on the Energy Gap of the Materials. So colour of the Emitted Light depends on the type of Material used.

GaAs - Infrared Radiation (Invisible)

GaP - Red or Green

GaAsP - Red or Yellow.

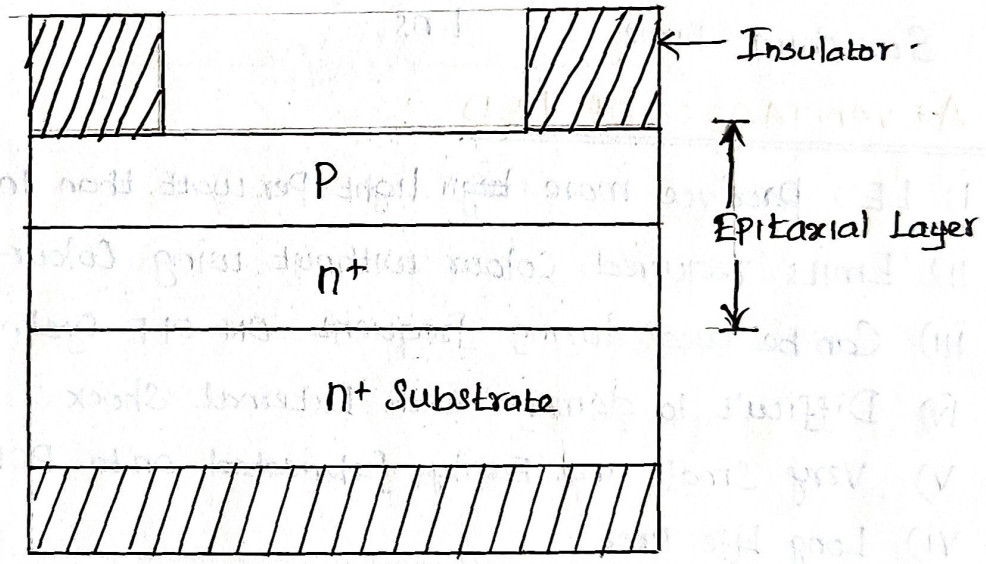


Fig. 2 Planner Surface emitting LED.

QUANTUM EFFICIENCY OF LED

It specifies the Efficiency of the Conversion of Electrical Energy into Emitted Optical Energy.

- It is defined as the ratio of light Output to Electrical input Power

$$\eta = \frac{P_{out}}{P_{in}}$$

ILD

When emitted light is coherent i.e., Monochromatic, then the diode is called as Injection Laser Diode (ILD)

ILD ADVANTAGES :

i) ILD has shorter rise time than LED.

ii) ILD is more suitable for wide-bandwidth and High data Rate applications

DISADVANTAGES :

i) More Temperature dependent

1. LED SPECIFICATIONS

Voltage levels	:	1.5 to 3.3V
Current	:	10 - 100 mA
Power	:	10 - 150 mW
Life time	:	more than 1,00,000 hours
Switching Time	:	1 ns

2. ADVANTAGES OF LED :

i) LED produce more light per watt than Incandescent bulbs.

ii) Emits required colour without using colour Filters

iii) Can be used during frequent ON-OFF cycling

iv) Difficult to damage with External shock.

v) Very small and Easily fabricated on to PCBs.

vi) Long life time.

3. DISADVANTAGES OF LED :

i) Depends on Ambient Temperature of Operature

ii) Correct Current should be supplied to LEDs.

iii) Low Efficiency.

4. APPLICATIONS OF LED :

i) Remote control CTVs, VCRs

ii) Lighting, Indicators, Electronic Panels.

iii) Devices, Medical Applications

iv) Toys, Burglar Alarms, Multimeters, Digital Meters

v) Opto isolators and opto couplers.

LASER DIODE

LASER Stands for Light Amplification by Stimulated Emission of Radiation. LASERS are used to convert the electrical signal to Light Signal.

– Similar to LED, Laser diodes are a form of PN Junction diode with a thin depletion ~~Layer~~ Region where electrons and holes collide to Create Light photons during Forward Bias.

* The only difference is that the active part of depletion Region is Very Narrow to increase Carrier Concentration.

The ends of this narrow active Region are highly polished to act as Mirrors so as to form a Resonant Optical Cavity.

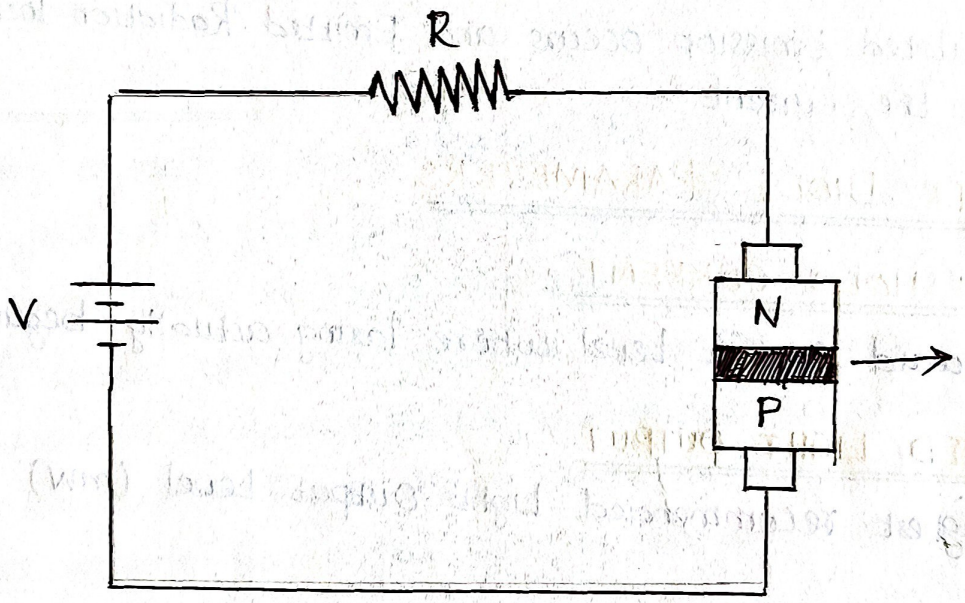


Fig. 1. Laser diode Structure.

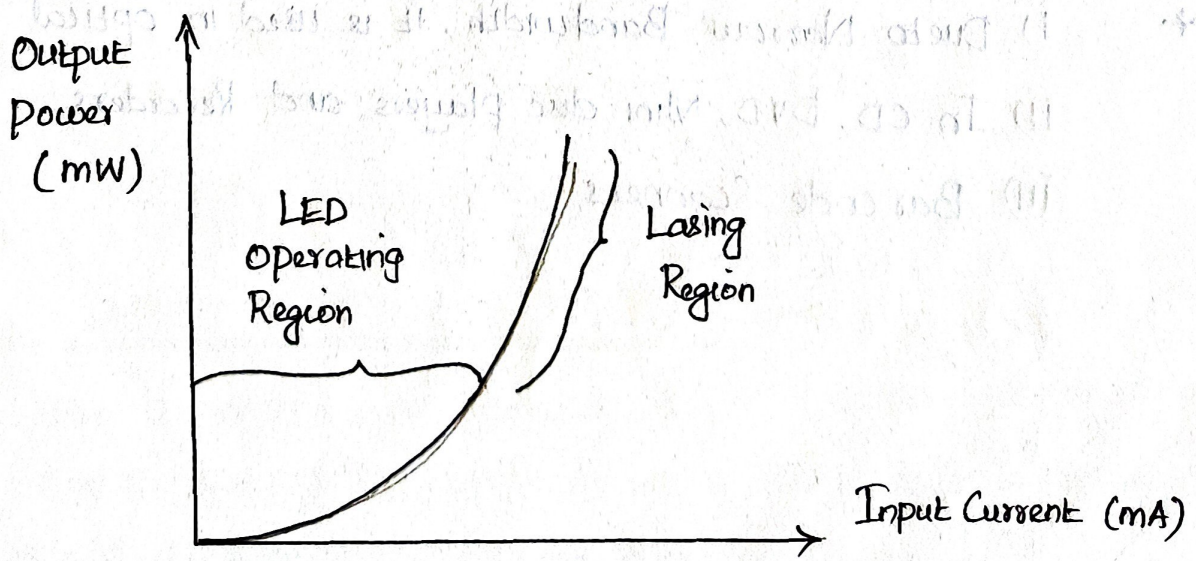


Fig. 2. Laser Diode Characteristics

The forward Current Level is also increased to the point where Current density reaches a critical level to achieve inversion i.e, there are more holes than electrons in Conduction Band and more electrons than holes in the Valence Band

- Such a large population of electrons and holes combine to release Photons, which intern Collide with electrons and holes to stimulate Production of more photons.

Thus laser action occurs and photons are able to travel back and forth from one end of Active Region to other. This triggers the Production of more and more photons in Sync with themselves producing Coherent Light Energy.

* All the photons of Laser have same Frequency and phase and hence it is called "Coherent". At limiting Current density, Stimulated Emission occurs and Emitted Radiation increases Linearly with the Current.

LASER DIODE PARAMETERS.

1. **THRESHOLD CURRENT :**
   Forward Current Level where lasing actually begin to occur.

2. **RATED LIGHT OUTPUT :**
   Highest recommended Light Output Level (mW)

APPLICATIONS :

* i) Due to Narrow Bandwidth, it is used in optical Systems
  ii) In CD, DVD, Mini disc players and Recorders
  iii) Bar code Scanners.

ZENER DIODE

In ordinary PN diode, the doping is light. So the Breakdown Voltage is high. If the P and N regions are heavily doped, then Breakdown Voltage can be reduced.

– When the Reverse voltage reaches the Breakdown Voltage, the Current through the junction and the power dissipation at the junction will be high

Due to large Amount of Current, there is possibility of damaging the diode, therefore the diodes are designed with adequate power dissipation Capability to operate in the Breakdown Region. The diode designed with such specification is called 'Zener diode' which is heavily doped than ordinary diode.

ZENER EFFECT :

When doping is heavy, the electric field at the junction will be very high even at Low Reverse Voltage. The electrons in Covalent Bonds break away from the bonds. This effect is called as 'Zener Effect'

– A diode which exhibits the Zener Effect is called Zener diode. Zener diode is a Reverse biased heavily doped diode which operates in the Breakdown Region. Zener diodes are designed to operate at Voltages ranging from a few Volts to several Hundred Volts.

SYMBOL

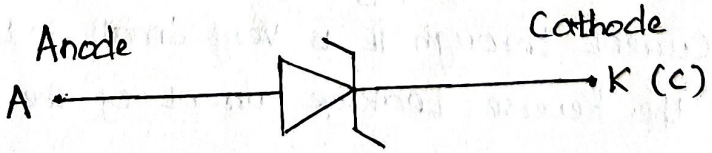


Fig. 1. Symbol of Zener diode

V-I CHARACTERISTICS OF DIODE

When Zener diode is forward biased, the Zener diode operation is similar to that of ordinary PN diode. Zener diode is specially designed to operate in the Reverse Bias Condition.

When the Reverse Voltage (V_R) is less than the Reverse Breakdown Voltage (V_Z), the diode carries Reverse Saturation Current $V_R < V_Z$

- When the Reverse Voltage is greater than the Reverse Breakdown Voltage, the Current through the diode increases rapidly and the Voltage across the diode remains Constant. $V_R * V_Z$

* Usually Zener diode is operated in the Reverse Breakdown Region. Due to this property, Zener diode is used for Providing Constant Voltage Source in 'Voltage Regulators'

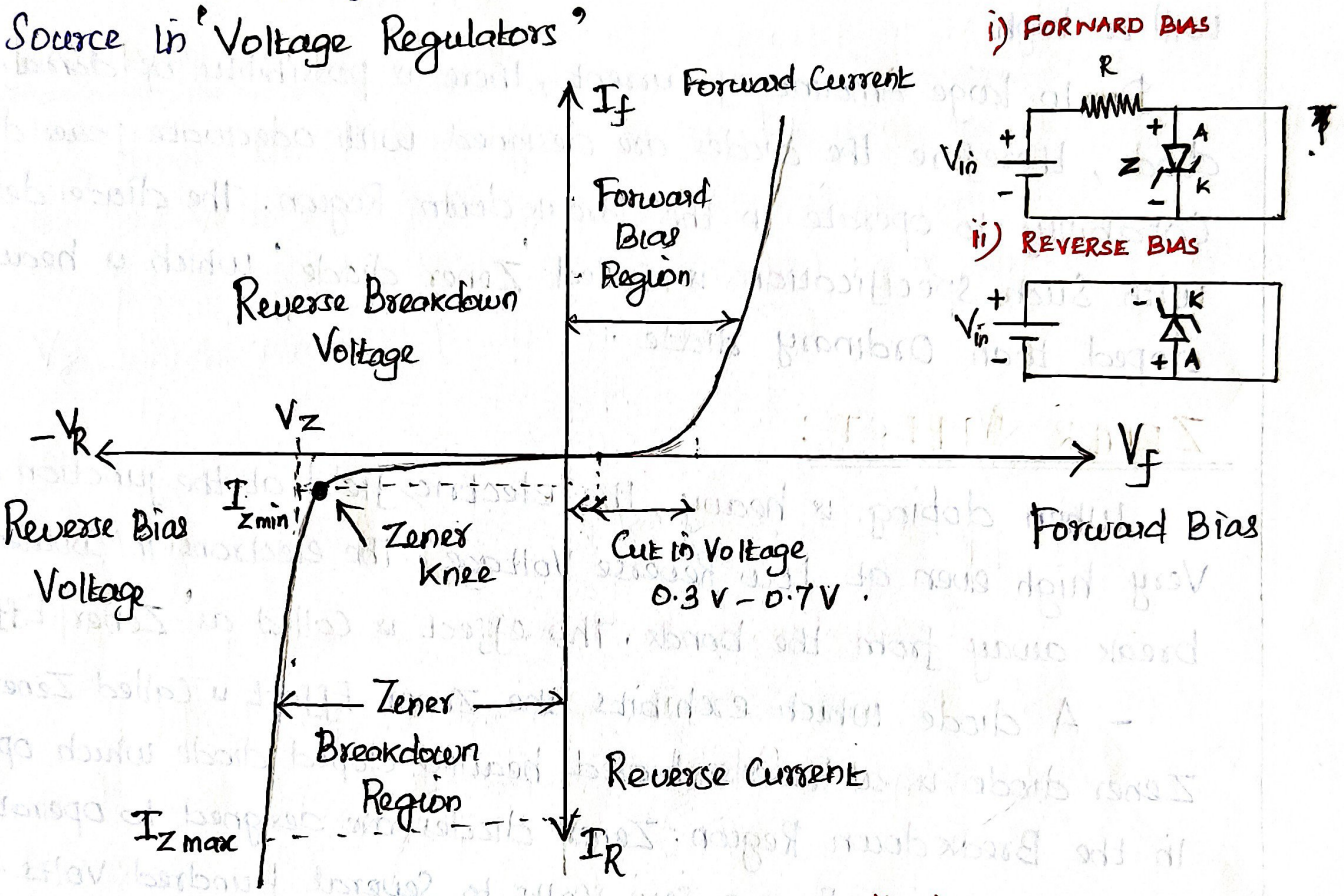


Fig. 2 V-I characteristics of Zener diode

When the Reverse Voltage applied to a Zener diode is increased, initially the Current through it is very small, in the order of few μA or less. This is the Reverse Leakage Current of the diode 'I_o'

KNEE

At Certain Reverse Voltage, the Current through Zener diode increases rapidly. This change from a Low Value to Large Current is very Sharp. This Sharp change in reverse characteristics is called 'Knee of the Curve'

At the Knee Voltage V_{knee}, the breakdown occurs. The Reverse Bias Voltage at which the breakdown occurs is called 'V_Z' 'Zener Breakdown Voltage'

The Current Corresponding to the Knee point is Called 'Zener Knee Current' denoted as I_{knee}.

- As Current is Increased, the power dissipation also increases ($P_z = V_z I_z$) If this power dissipation increases beyond Certain Value, the diode may get damaged.

* The maximum Current at which a Zener diode can operate Safely is Called 'Zener Maximum Current' I_{Zmax}.

EQUIVALENT CIRCUIT OF ZENER DIODE

When the Breakdown occurs I_z increases from I_{Zmin} to I_{Zmax} and the Voltage across Zener diode remains Constant

- Ideally the Zener diode is indicated by a battery of Voltage V_z which remains fairly Constant.

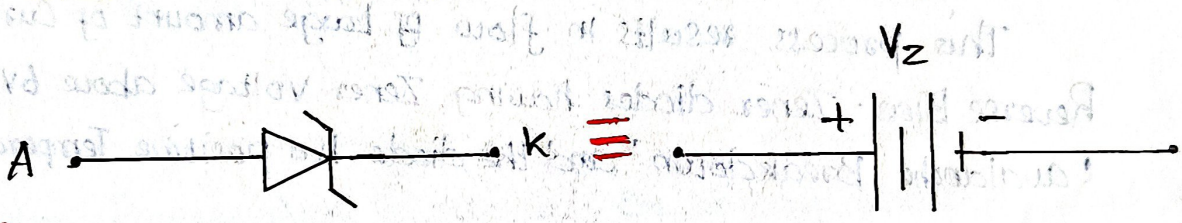


Fig. 3. Equivalent Circuit of Zener diode.

Fig. 3 Shows the equivalent Circuit of Zener diode. In Reverse Bias, the Resistance is Called 'Dynamic Resistance r_z' of the Zener diode.

ZENER RESISTANCE : (r_z)

The Ratio of change in Zener Voltage to the change in Zener Current is Called 'Zener Resistance r_z'

$$r_z = \frac{\Delta V_z}{\Delta I_z} = \frac{1}{\left(\frac{\Delta I_z}{\Delta V_z}\right)} = \frac{1}{\text{Slope of Reverse Characteristics}}$$

BREAKDOWN MECHANISMS IN ZENER DIODE

There are two types of Mechanisms due to which Breakdown Occurs. They are

1. Zener Breakdown
2. Avalanche Breakdown.

1. AVALANCHE BREAKDOWN

When the Reverse Bias Voltage is Increased, the electric field across the junction. Thermally generated Carriers Crossing the junction acquire a large amount of Kinetic Energy from this field.

- The Velocity of these charge Carriers Increases and these electrons disrupt Covalent Bond by colliding with Immobile Ions and create 'electron-hole Pairs'

* This new charge Carriers again acquire Sufficient Energy from the field and collide with other Immobile Ions and generate further 'electron-hole Pairs'. This process Continues and results in generation of avalanche of charge Carriers within a short time. This Mechanism of Carrier generation is Called as 'Avalanche Multiplication'

This process results in flow of Large amount of Current at the Reverse Bias. Zener diodes having Zener Voltage above 6V exhibit 'avalanche Breakdown' and the diode has positive Temperature Coefficient.

2. ZENER BREAKDOWN :

When P and N regions are heavily doped, Strong electric field is Created which results in direct rupture of Covalent Bonds. Hence new 'electron-hole Pairs' are generated and the Reverse Current begins to Increase.

- This process occurs at a Reverse Bias below 6V. Due to Heavy doping, the depletion width becomes Very Small and the electric field across the depletion Region becomes very high of the order of 10^7 V/m. Thus 'Zener Breakdown' occurs.

* For Lightly doped diodes, the Breakdown Voltage is high and it is mainly due to 'Avalanche Multiplication'. Thus in zener diode, Breakdown occurs both in Lower and Higher Breakdown Voltages i.e, both 'Avalanche and Zener Breakdown' occurs. Such a diodes are Called 'Zener Diode'

TEMPERATURE COEFFICIENT OF ZENER DIODE

The percentage change in the Zener Voltage V_z for every °C rise / Fall in Temperature is called Temperature Coefficient (TC) of a zener diode

$$TC = \frac{\Delta V_z}{V_z (T_1 - T_0)} \times 100 \ \%/^\circ C$$

T_1 - Change in Temperature

T_0 - Initial Temperature

If $V_z < 6V$, the temperature Coefficient is Negative

$V_z > 6V$, the temperature Coefficient is Positive

ZENER DIODE AS VOLTAGE REGULATOR

When Reverse Bias is applied, the Voltage across the diode remains Constant and the Current through the diode Increases.

- The Voltage across the Zener diode acts as a Reference Voltage and the diode can be used as 'Voltage Regulator'.

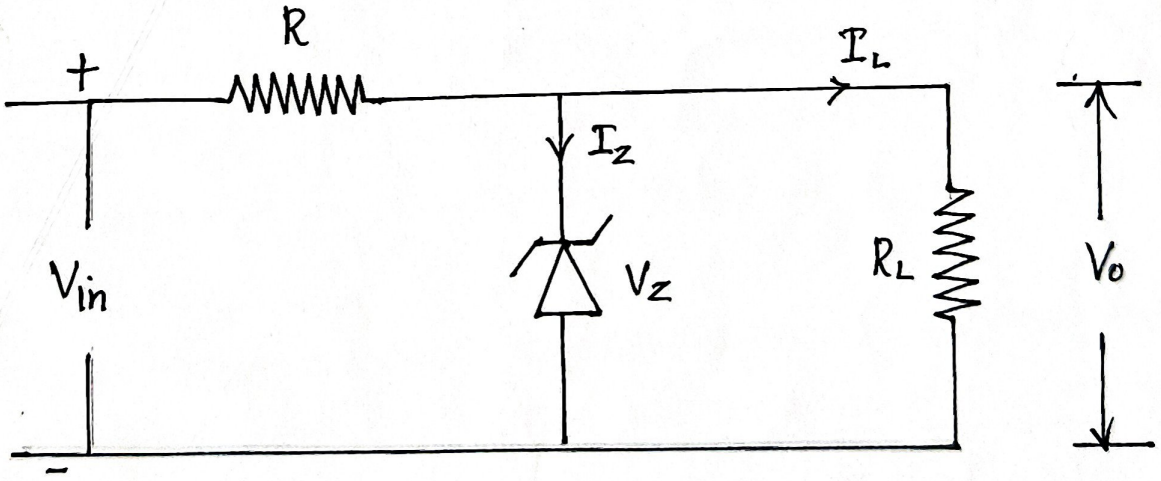


Fig.1. Zener diode act as Voltage Regulator.

In the fig.1. shown, the Load Resistance should be be provided with Constant Voltage.

Zener diode is Reverse Biased and if the Input Voltage is not less than Zener Breakdown Voltage V_Z ($V_{in} > V_Z$) then the Voltage across the diode will be Constant and thus the Load Voltage is also Constant.

APPLICATIONS OF ZENER DIODE

1. Voltage Regulators
2. Zener Limiters to clip the unwanted Portion of the Voltage waveform
3. Over Voltage Protection.

UNIT- II TRANSISTORS

The BJT is a main building Block of all Modern electronic Systems. It is a three terminal (**Emitter, Base and Collector**) Semiconductor device in which the operation depends on the Interaction of both Majority and Minority Carriers and hence the name **'Bipolar'**.

BJT (Bipolar Junction Transistor), ~~the name 'Bipolar'~~ Transistor means Transfer Resistor Signals from Low Resistance Circuit into High Resistance Circuit

* In Communication Systems, it is used as a primary Component in the 'Amplifier'. An Amplifier is a circuit that is used to increase the Strength of an AC signal

- In Digital Computer Electronics, the 'BJT' is used as a high speed Electronic Switch that is capable of Switching between two operating States (open and closed).

TRANSISTORS

A BJT has a Very Important Property that can raise the Strength of a weak signal. This property is Called 'Amplification'. Because of this property, the transistor is one of the most widely used Semiconductor devices.

* the Amplification in the transistor is achieved by Passing the Signal from a region of Low Resistance to a Region of High Resistance. This Concept of transfer of resistance has given the name 'Transistor' (Transfer - Resistor)

APPLICATIONS OF TRANSISTORS :

The transistors are used in digital Computers, Satellites, Mobile phones and other Communication Systems etc,

CLASSIFICATION OF TRANSISTORS

There are two types of Transistors

1. Unipolar Junction Transistor
2. Bipolar Junction Transistor.

1. UNIPOLAR JUNCTION TRANSISTOR :

In Unipolar Transistor the current conduction is only due to one type of carriers, (i.e.) Majority carriers. These transistors are commonly known as Field Effect Transistor (FET).

* In FET, the current flow is controlled by an Electric Field setup in the device by an externally applied voltage, hence the name 'field Effect'

- FET is a voltage operated device (i.e., Output current is controlled by input voltage.)

The FET's are categorised as

i) Junction Field Effect Transistor (JFETs)
ii) Metal Oxide Semiconductor FETs (MOSFETs)
iii) Metal - Semi Conductor FET (MESFET)

2. BIPOLAR JUNCTION TRANSISTOR

In Bipolar junction Transistor, the current conduction is due to Both the types of charge carriers, holes and Electrons. Hence it is called Bipolar Junction Transistor (BJT) or Transistor.

- BJT is a current operated device (i.e., Output current is controlled by Input current).

* It is classified into

i) NPN Type
ii) PNP Type.

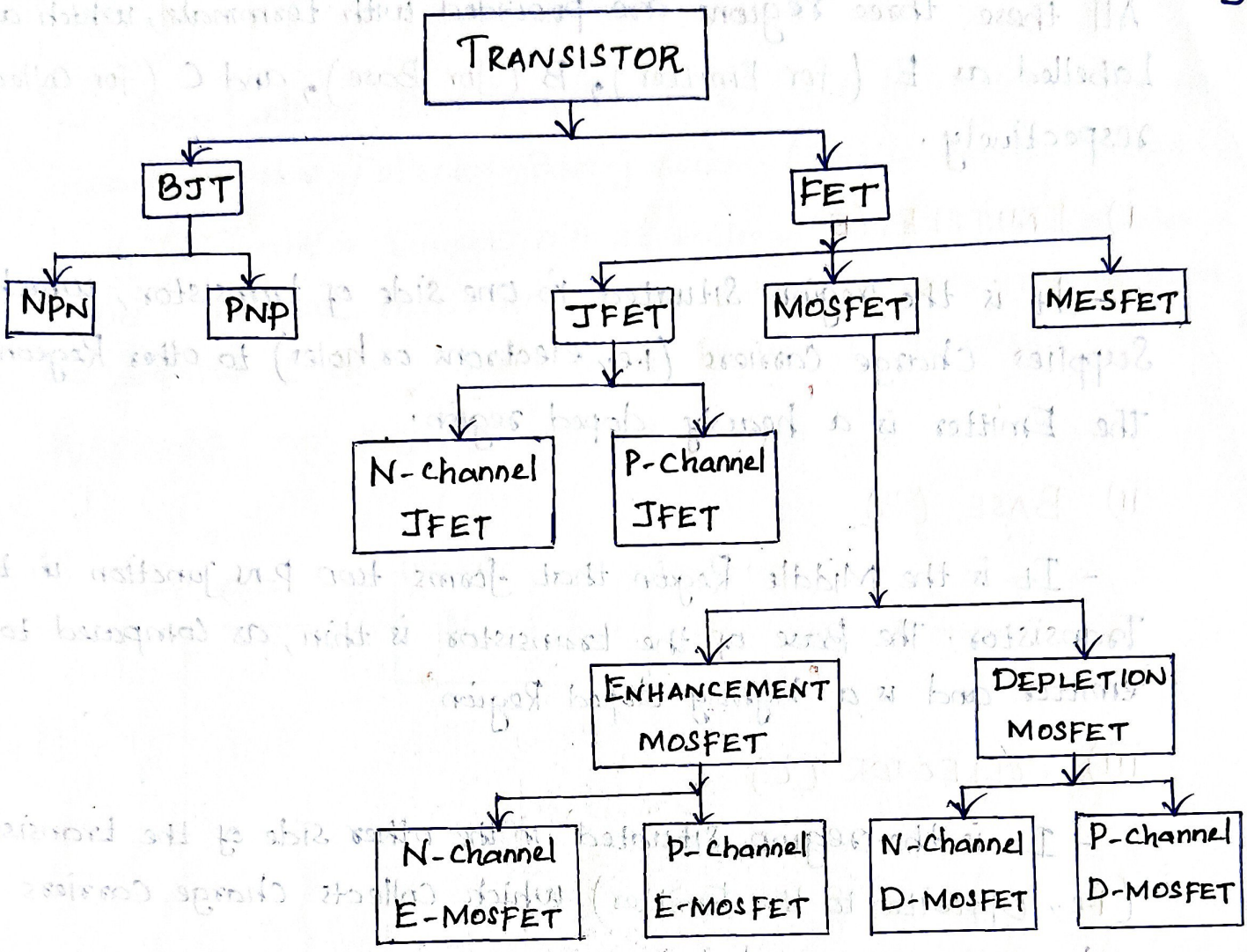


Fig.1. classification of Transistors.

BIPOLAR JUNCTION TRANSISTOR (BJT)

1. TRANSISTOR CONSTRUCTION

A transistor consists of two PN junctions formed by sandwiching either P-Type or N-type semiconductor between a pair of opposite types.

* There are two types of transistors, namely

i) N-P-N Transistor

ii) P-N-P Transistor.

A Bipolar transistor has three regions known as Emitter, Base and Collector

All these three regions are provided with terminals, which are Labelled as E (for Emitter), B (for Base), and C (for Collector) respectively.

i) EMITTER (E)

- It is the region situated in one side of transistor, which supplies charge carriers (i.e., electrons or holes) to other Regions The Emitter is a 'heavily doped region'

ii) BASE (B)

- It is the Middle Region that forms two P-N junction in the Transistor. The Base of the transistor is thin, as compared to the emitter and is a 'Lightly doped Region'

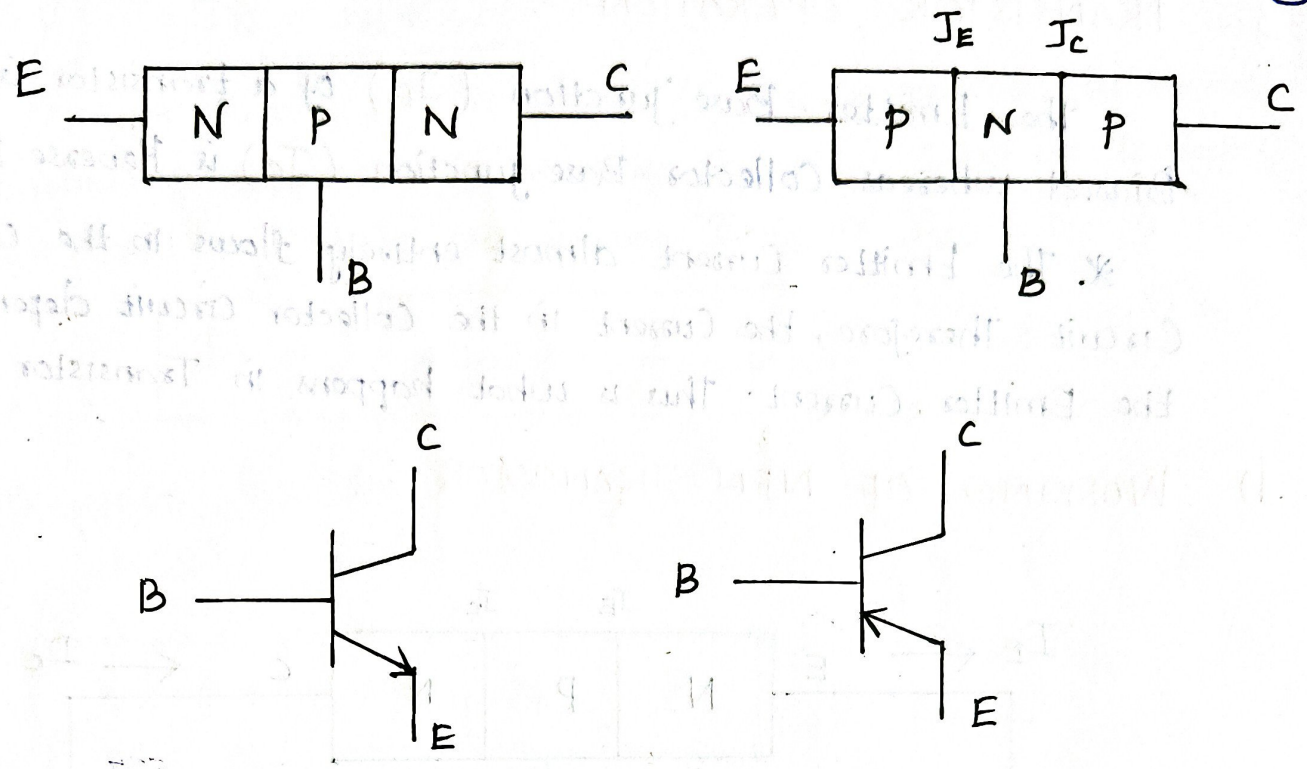
iii) COLLECTOR (C)

- It is the region situated in the other side of the transistor (i.e., Opposite to the Emitter) which collects charge carriers (i.e., electrons or holes).

* the Collector of a transistor is always larger than the Emitter and Base of a Transistor.

- The doping Level of the collector is intermediate between the Heavy doping of Emitter and Light doping of the Base (Moderately doped)

- The Transistor has three Regions, namely; Emitter, Base, Collector. The Base is much thinner than the Emitter, While Collector is wider than Both.
- → The Emitter is Heavily doped so that it can inject a Large Number of charge Carriers into the Base
- → The Base is Lightly doped and Very thin; it passes most of the Emitter injected Charge Carriers to the Collector.
- → the Collector is Moderately doped.



i) NPN Transistor Symbol. ii) PNP Transistor Symbol.

Fig. 2. STANDARD TRANSISTOR SYMBOL

The transistor has two junctions i.e, it is like two diodes. The junction between Emitter and Base may be Called 'Emitter - Base diode (or) Emitter diode (or) Emitter junction (J_E)'

- The junction Between Base and Collector may be Called 'Collector - Base diode (or) Collector diode (or) Collector Junction (J_C)'

- The Emitter diode is always Forward Biased whereas the Collector diode is always Reverse Biased.

2. MODES OF OPERATION :

In order to Transistor properly as an Amplifier, the two PN junctions should be Correctly Biased with External Voltages.

* Depending upon External Bias Voltage Polarities used, the transistor works in one of the Three Regions i) Active Regions ii) Cut-off Region and iii) Saturation Region.

i) ACTIVE REGION : J_E Forward Bias ; J_C Reverse Bias
ii) SATURATION REGION : J_E Forward Bias ; J_C Forward Bias
iii) CUT-OFF REGION : J_E Reverse Bias ; J_C Reverse Bias.

3. TRANSISTOR OPERATION

The Emitter-Base junction (J_E) of a transistor is forward Biased whereas Collector-Base junction (J_C) is Reverse Biased.

* The Emitter Current almost entirely flows in the Collector Circuit. Therefore, the Current in the Collector Circuit depends upon the Emitter Current. This is what happens in Transistor.

i) WORKING OF NPN TRANSISTOR :

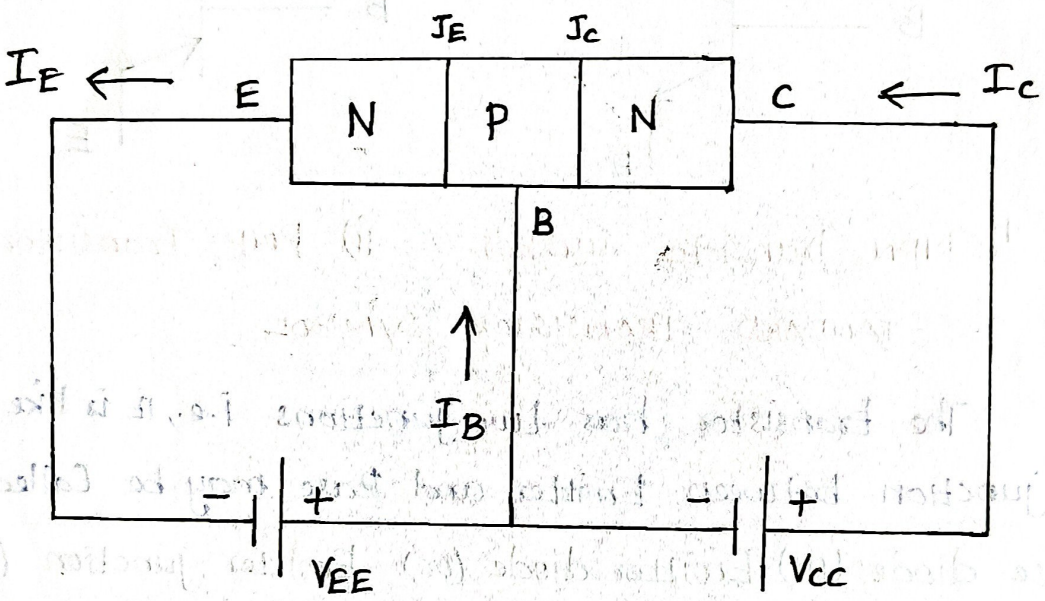


Fig. 3. N-PN Transistor

The fig. 3 Shows the NPN transistor with forward Bias to Emitter-Base junction (J_E) and Reverse Bias to Collector-Base junction (J_C)

* The forward Bias Causes the electrons in the N-type Emitter to flow through the P-Type Base, they tend to Combine with holes

- As the Base is Lightly doped and Very thin, therefore, only a few electrons (less than 5%) Combine with holes to Constitute Base Current 'I_B'. The remainder (More than 95%) Cross over into the Collector Region to Constitute Collector Current 'I_C'

- In this way, almost the entire Current flows in the Collector Circuit. The Emitter Current is Sum of Collector Current and Base Current.

$$I_E = I_B + I_C$$

The Collector Current is Comprised of two components, the Majority and Minority Carriers. The Minority Current is called the Leakage Current and is given by the Symbol I_{CBO} or I_{CO}.

$$I_C = I_{C\,majority} + I_{CO\,Minority}$$

ii) WORKING OF PNP TRANSISTOR

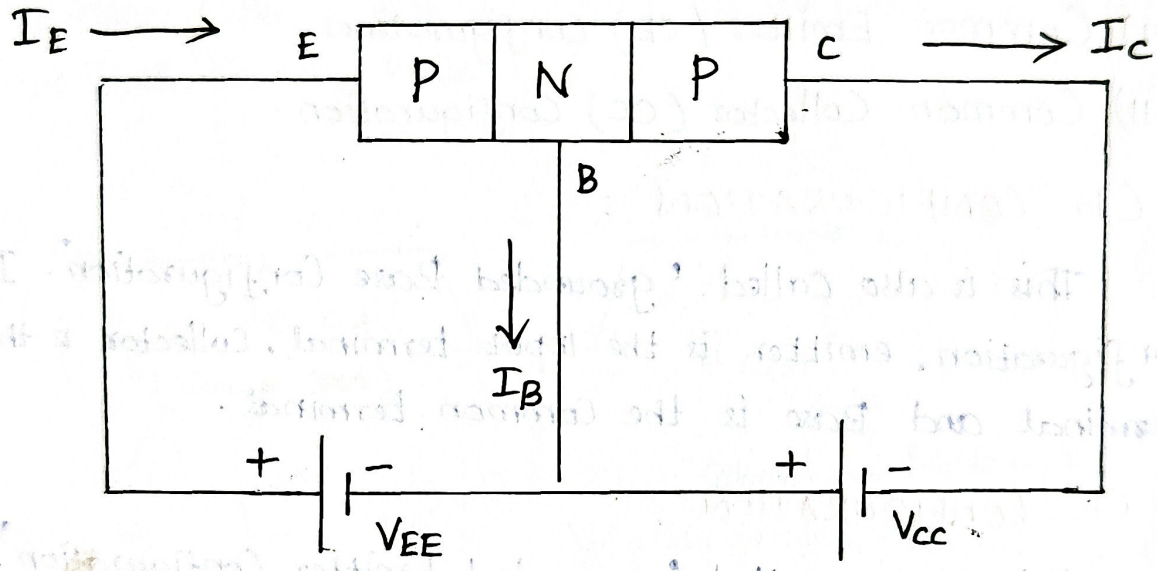


Fig. 4. PNP Transistor

Fig.4 Shows the PNP Transistor with forward Bias to Emitter-Base junction (I_E) and Reverse Bias to Collector-Base Junction (I_C).

* The forward Bias Causes the holes in the P-Type Emitter to flow towards the Base. This Constitutes the Emitter Current (I_E)

→ As these holes flows through the N-Type Base, they tends to Combine with Electrons. As the Base is "Lightly doped" and very thin, therefore only few holes (less than 5%) Combine with electrons to Constitute Base Current (I_B)

The remainder (More than 95%) Cross over into the Collector region to Constitute Collector Current (I_C). In this way, almost the entire Current flows in the Collector Circuit. "The Current Conduction within PNP Transistor is by 'holes'"

TYPES OF CONFIGURATION

When a transistor to be connected in a circuit, one terminal is used as an input terminal, the other terminal is used as an output terminal and the third terminal is common to the input and output.

* Depending upon the input, output and common terminal, a transistor can be connected in three configurations. They are

i) Common Base (CB) Configuration.
ii) Common Emitter (CE) Configuration.
iii) Common Collector (CC) Configuration.

i) CB CONFIGURATION :

This is also called 'grounded Base Configuration'. In this configuration, emitter is the input terminal, collector is the output terminal and Base is the common terminal.

ii) CE CONFIGURATION :

This is also called 'grounded Emitter Configuration'. In this configuration, Base is the input terminal, Collector is the output terminal and Emitter is the common terminal.

iii) CC CONFIGURATION :

This is also called 'grounded Collector Configuration'. In this configuration, Base is the input terminal, Emitter is the output terminal and Collector is the common terminal.

COMMON BASE CONFIGURATION

In this Circuit arrangement, input is applied between Emitter and Base and Output is taken from Collector and Base.

- Here, Base of the Transistor is Common to Both Input and Output Circuits and hence the name 'Common Base Connection'.

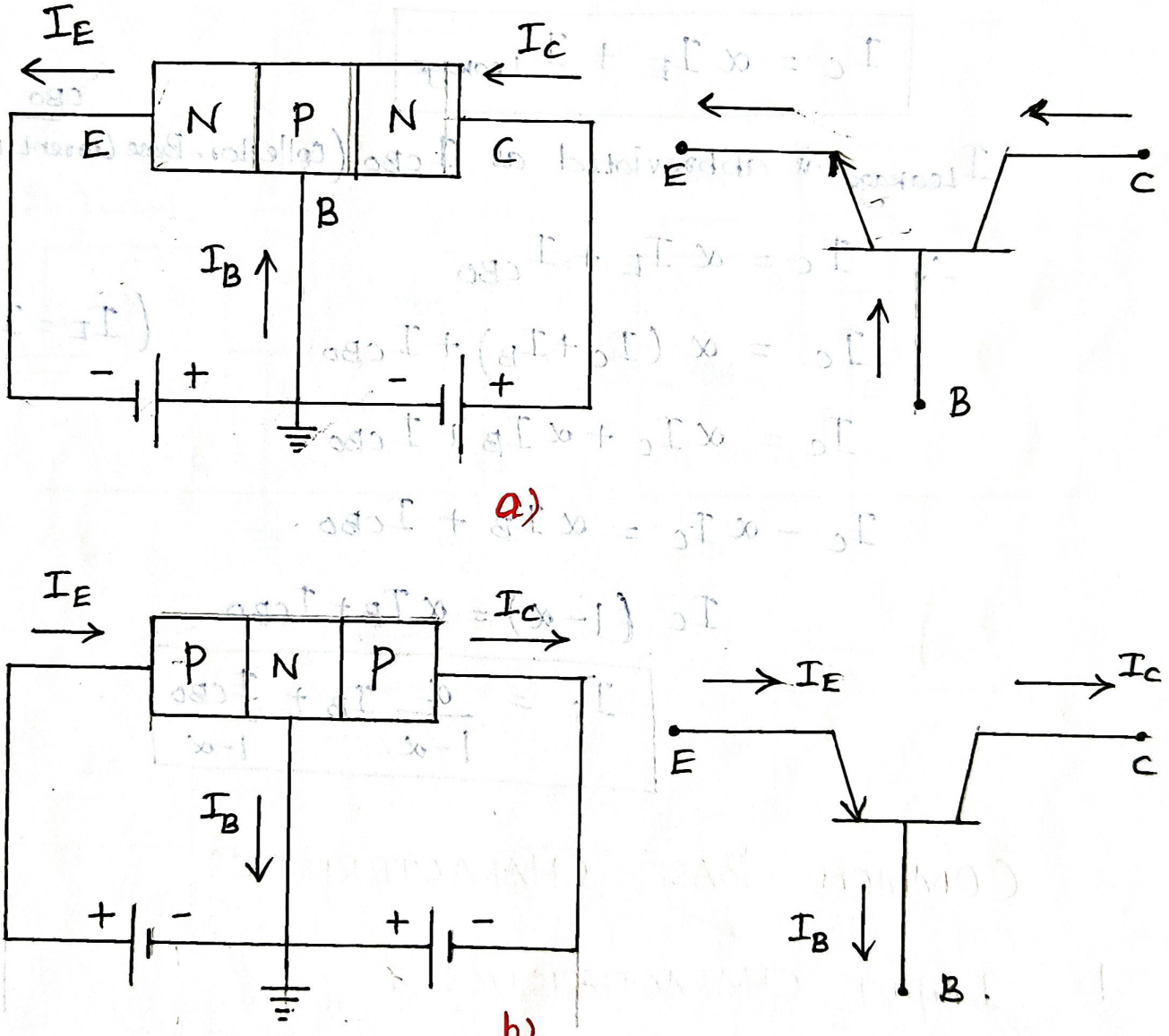


Fig 1. Notation and Symbols used with Common-Base Configuration
a) NPN Transistor b) PNP Transistor.

* CURRENT AMPLIFICATION FACTOR (α):

I_E is the ratio of output Current to Input Current.

$$\alpha = \frac{I_C}{I_E}$$ or $$\alpha = \frac{\Delta I_C}{\Delta I_E}$$

α is less than Unity (ranges from 0.9 to 0.99).

EXPRESSION FOR COLLECTOR CURRENT :

The whole of Emitter Current (I_E) doesnot reach the Collector. The part of Emitter Current reaches the Collector terminal i.e., 'αI_E'

The Leakage Current $I_{leakage}$ is dueto movement of Minority Carriers across the Base-Collector Junction on account of it being Reverse Biased. The total Collector Current (I_C) is

$$\boxed{I_C = \alpha I_E + I_{Leakage}}$$

$I_{Leakage}$ is abbreviated as I_{CBO} (Collector-Base Current with Emitter Open)

$$\therefore \quad I_C = \alpha I_E + I_{CBO}$$

$$I_C = \alpha (I_C + I_B) + I_{CBO} \qquad (I_E = I_C + I_B).$$

$$I_C = \alpha I_C + \alpha I_B + I_{CBO}.$$

$$I_C - \alpha I_C = \alpha I_B + I_{CBO}.$$

$$I_C (1-\alpha) = \alpha I_B + I_{CBO}$$

$$\boxed{I_C = \frac{\alpha}{1-\alpha} I_B + \frac{I_{CBO}}{1-\alpha}}$$

COMMON BASE CHARACTERISTICS

1. INPUT CHARACTERISTICS :

The Input Characteristics for the Common-Base Configuration relates an Input Current (I_E) to an Input Voltage (V_{BE}) for Various levels of Output Voltage (V_{CB}) is shown in fig. 2.

1) The Emitter Current (I_E) increases rapidly after the Cut-in Voltage with Small increase in Emitter-Base Voltage (V_{BE})
   - It indicates that Input Resistance is Very Small.

DYNAMIC INPUT RESISTANCE (r_i) :

The Input Resistance is the ratio of change in Emitter-Base Voltage (ΔV_{BE}) to the Corresponding change in Emitter Current (ΔI_E) at Constant Collector-Base Voltage (V_{CB}).

Dynamic Input Resistance, $$r_i = \left.\frac{\Delta V_{BE}}{\Delta I_E}\right|_{V_{CB}\ \text{Constant}}$$

ii) There is a Slight increase in Emitter Current (I_E) with Increase in (V_{CB})

- Depletion Region width at the Emitter-Base Junction (J_E) (i.e. Emitter Diode) is Small because it is forward Biased, whereas the Depletion Region width at the Collector-Base Junction (J_C) is more because it is Reverse biased.

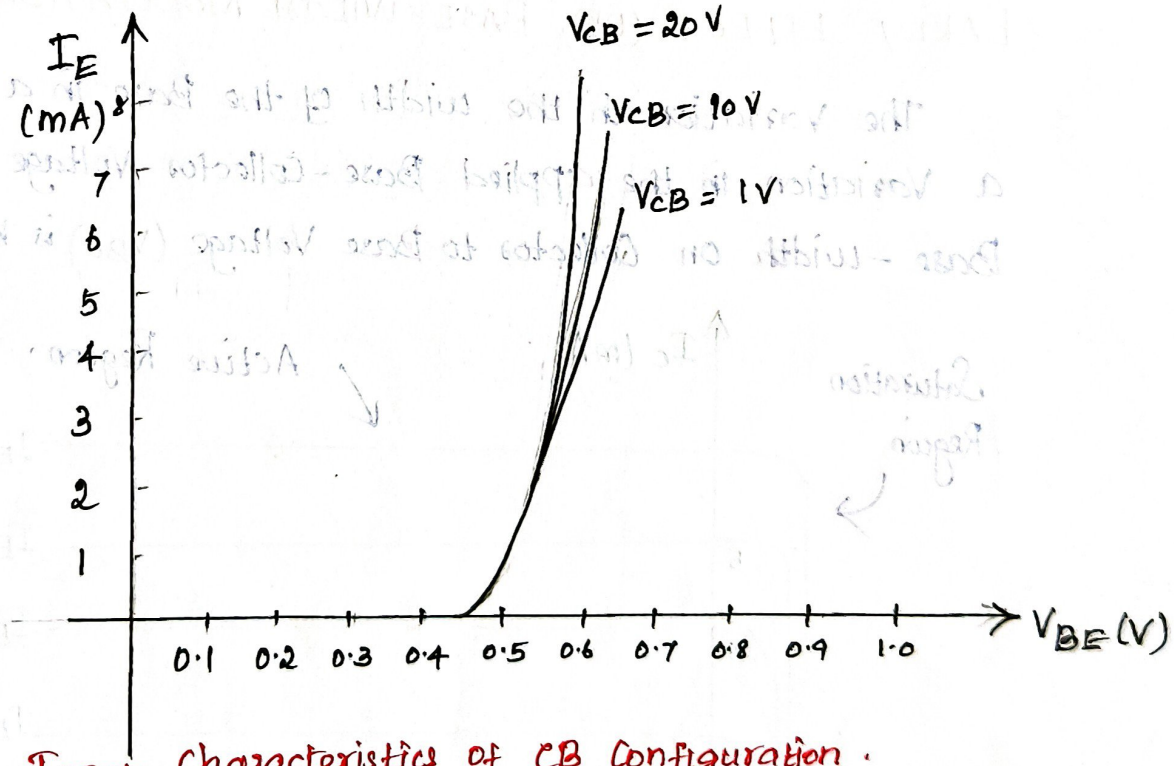


Fig. 2. Input characteristics of CB configuration.

2. OUTPUT CHARACTERISTICS :

The Output characteristics relates an Output Current (I_C) to an Output Voltage (V_{CB}) for Various levels of Input Current (I_E)

- the Output has three Regions, i) Active Region ii) Cut-OFF Region and iii) Saturation Region as shown in fig. 3.

i) ACTIVE REGION :

In the active Region, the Base-Emitter junction (J_E) (Emitter diode) Forward biased, whereas the Collector-Base junction (J_C) (Collector diode) Reverse Biased.

* In the Active Region, the Collector Current (I_C) increases to a magnitude equal to that of Emitter Current (I_E)

$$I_C \simeq I_E$$

ii) SATURATION REGION :

In the Saturation Region, both Base-Emitter Junction (J_E) and Collector-Base Junction (J_C) are forward biased

- Sudden increase in the collector current (I_C) as the V_{CB} Increases towards `0V'

EARLY EFFECT (OR) BASE-WIDTH MODULATION :

The Variation in the width of the Base in a transistor due to a Variation in the applied Base-Collector Voltage (V_{BC}). The Base-width on Collector to Base Voltage (V_{BC}) is known as "Early EFFECT"

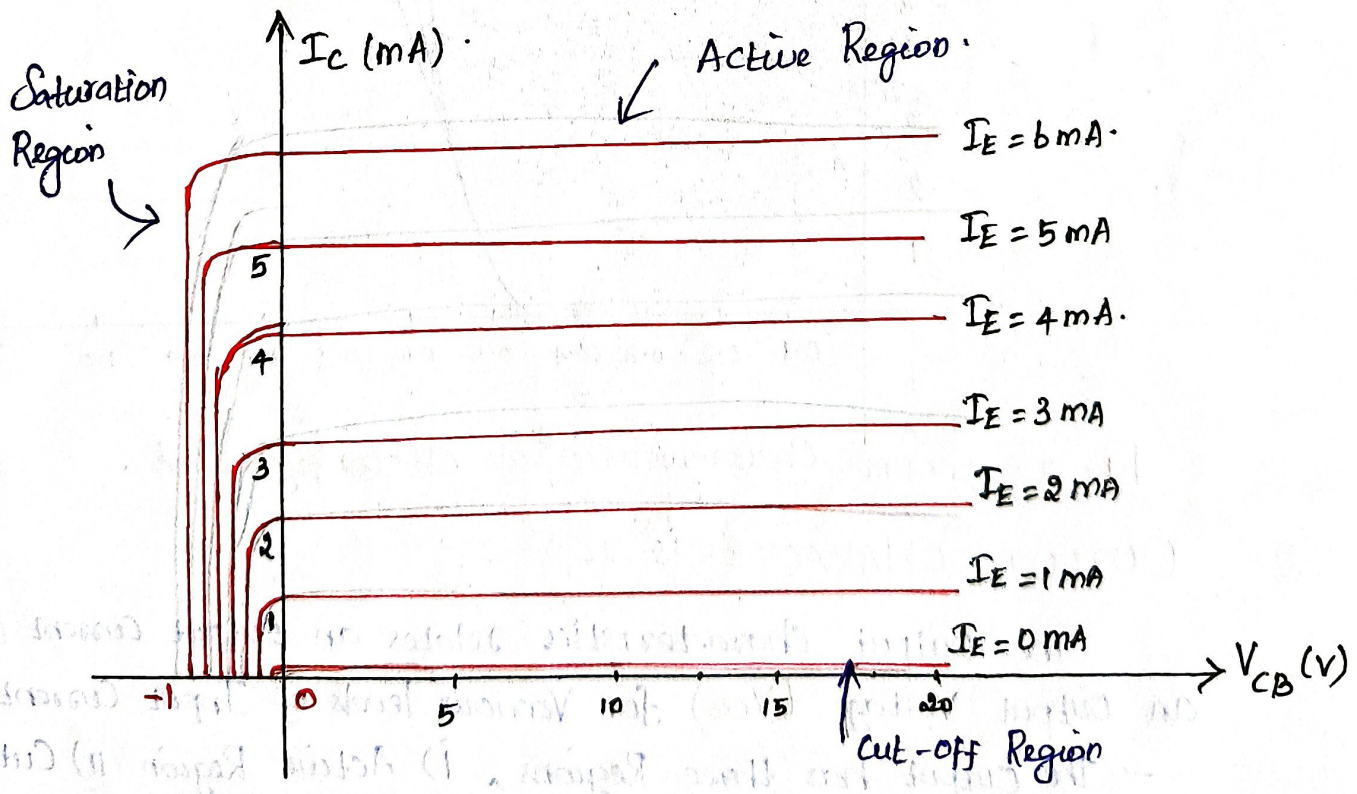


Fig. 3. Output Characteristics

iii) CUT-OFF REGION

If the emitter Current 'I_E' is Zero, the Collector Current (I_c) is the only due to Reverse Saturation Current (I_{CBO}) as shown in fig.4.

* This Current is Very Small in magnitude (μA or nA). The region below the Curve $I_E = 0$ is known as 'Cut-off Region' Where the Collector Current (I_C) is almost Zero

- In the Cut-off Region the Base-Emitter junction (Emitter Diode) 'I_E' and Collector-Base Junction (Collector diode) 'I_C' of a transistor are both Reverse Biased.

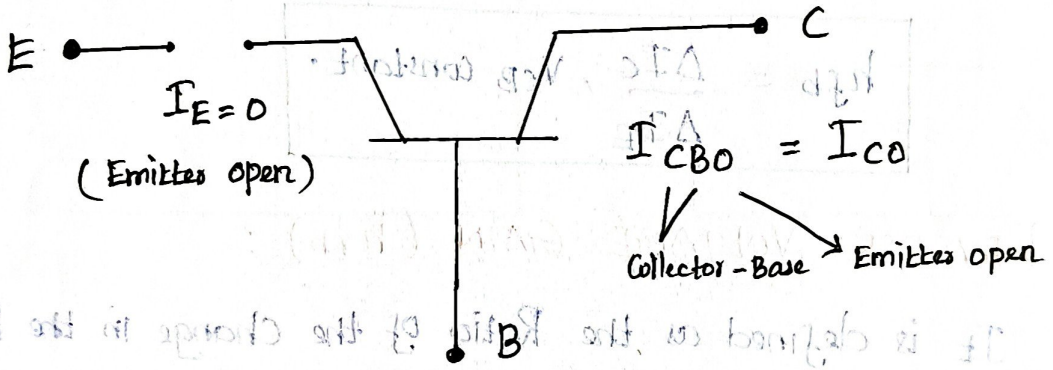


Fig.4. Reverse Saturation Current, I_{CBO}.

TRANSISTOR PARAMETERS

The Slope of the CB Characteristics will give the following Parameters. They are Commonly Known as Common-Base Hybrid parameters or 'h-Parameters'

i) INPUT IMPEDANCE (h_{ib})

It is defined as the Ratio of the change in Emitter Voltage (ΔV_{EB}) to the change in Emitter Current (I_E) with the V_{CB} Kept Constant.

$$h_{ib} = \frac{\Delta V_{BE}}{\Delta I_E}, \quad V_{CB} \text{ constant}$$

ii) OUTPUT ADMITTANCE (h_{ob}) :

It is defined as the Ratio of Change in Collector Current (ΔI_c) to the Corresponding Change in the Collector Voltage (V_{CB}) with the 'I_E' Kept Constant

$$h_{ob} = \frac{\Delta I_c}{\Delta V_{CB}}, \; I_E \text{ constant.}$$

iii) FORWARD CURRENT GAIN (h_{fb}) :

It is defined as a ratio of the change in the Collector Current (ΔI_C) to the Corresponding change in Emitter Current (ΔI_E) with the 'V_{CB}' Kept Constant.

$$h_{fb} = \frac{\Delta I_C}{\Delta I_E}, \; V_{CB} \text{ constant.}$$

iv) REVERSE VOLTAGE GAIN (h_{rb}) :

It is defined as the Ratio of the change in the Emitter Voltage (ΔV_{BE}) to the Corresponding change in Collector Voltage (V_{CB}) with the 'I_E' Kept Constant

$$h_{rb} = \frac{\Delta V_{BE}}{\Delta V_{CB}}, \; I_E \text{ constant.}$$

COMMON EMITTER CONFIGURATION

In this circuit arrangement, input is applied between Base and Emitter and, the Output is taken from Collector and Emitter.

- Here, Emitter of the transistor is common to both input and Output circuit and hence the name 'Common Emitter Connection'

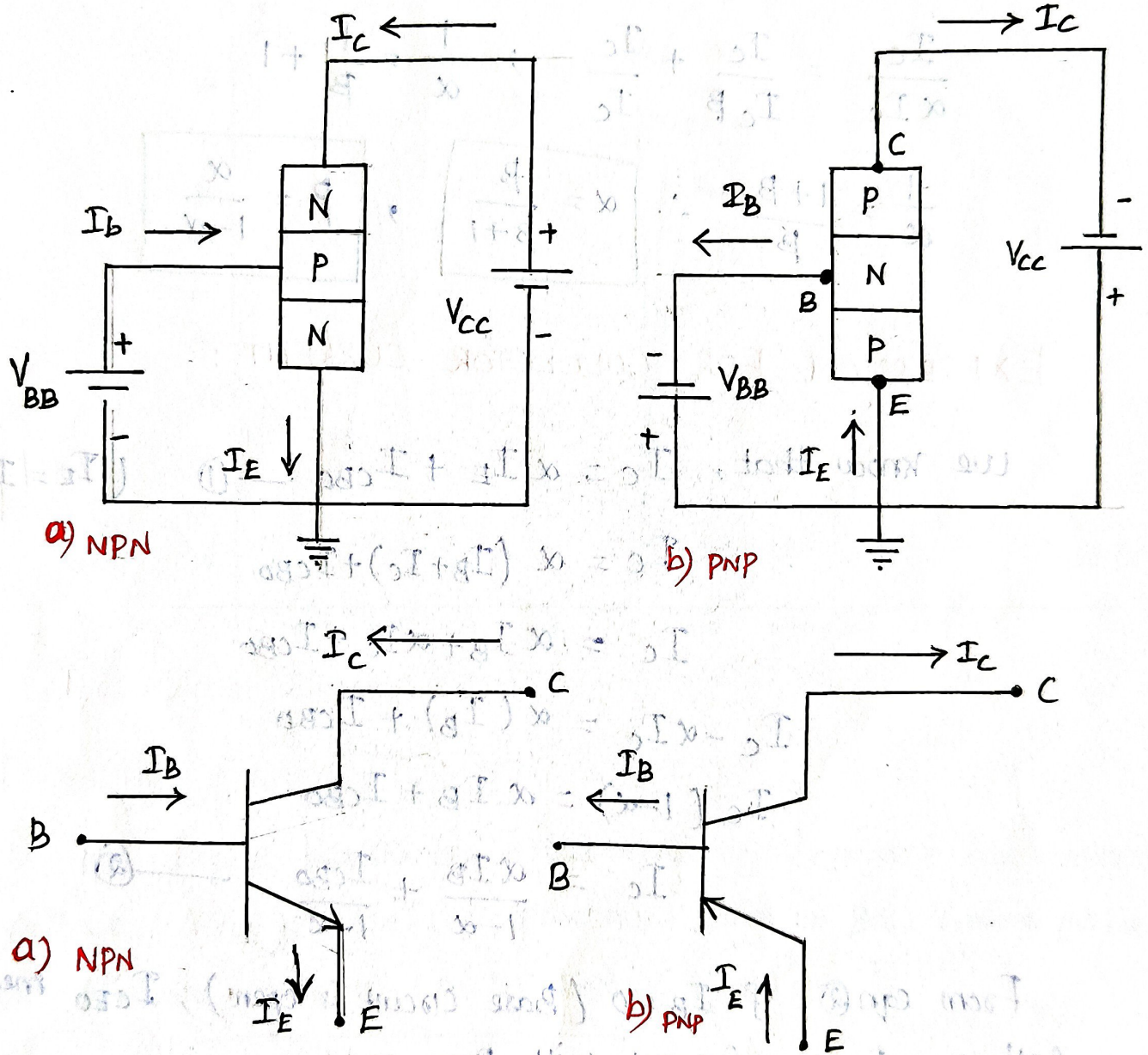


Fig. 1. Notation and Symbol used with the Common-Emitter Configuration

* BASE CURRENT AMPLIFICATION FACTOR (β):

It is defined as the Ratio of Change in Collector Current (ΔI_C) to the Change in Base Current (ΔI_B) is known as 'β'

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

RELATION BETWEEN α and β.

Using $\beta = \frac{I_C}{I_B}$ then $\boxed{I_B = \frac{I_C}{\beta}}$, $\boxed{I_E = \frac{I_C}{\alpha}}$

$$I_E = I_B + I_C$$

$$\frac{I_C}{\alpha} = \frac{I_C}{\beta} + I_C \quad \text{Dividing on both sides by } 'I_C'$$

$$\frac{I_C}{\alpha I_C} = \frac{I_C}{I_C \beta} + \frac{I_C}{I_C} \quad ; \quad \frac{1}{\alpha} = \frac{1}{\beta} + 1$$

$$\frac{1}{\alpha} = \frac{1+\beta}{\beta} \quad \therefore \boxed{\alpha = \frac{\beta}{\beta+1}}, \quad \boxed{\beta = \frac{\alpha}{1-\alpha}}$$

EXPRESSION FOR COLLECTOR CURRENT :

We know that, $I_C = \alpha I_E + I_{CBO}$ ——— ① $(I_E = I_B + I_C)$

$$I_C = \alpha (I_B + I_C) + I_{CBO}$$

$$I_C = \alpha I_B + \alpha I_C + I_{CBO}$$

$$I_C - \alpha I_C = \alpha (I_B) + I_{CBO}$$

$$I_C (1-\alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha I_B}{1-\alpha} + \frac{I_{CBO}}{1-\alpha} \quad \text{——— ②}$$

From eqn ②, if $I_B = 0$ (Base circuit is open), I_{CEO} meaning Collector-Emitter Current with Base open.

$$\boxed{I_{CEO} = \frac{I_{CBO}}{1-\alpha}} \quad \text{——— ④} \quad \text{eqn ④ in eqn ②.}$$

$$I_C = \frac{\alpha}{1-\alpha} I_B + I_{CEO}$$

$$\boxed{I_C = \beta I_B + I_{CEO}} \quad \left[\beta = \frac{\alpha}{1-\alpha}\right]$$

COMMON EMITTER CHARACTERISTICS

1. INPUT CHARACTERISTICS :

The Input Characteristics for the Common-Emitter Configuration relates an Input Current (I_B) to an Input Voltage (V_{BE}) for Various levels of Output Voltage (V_{CE}) as shown in fig. 2

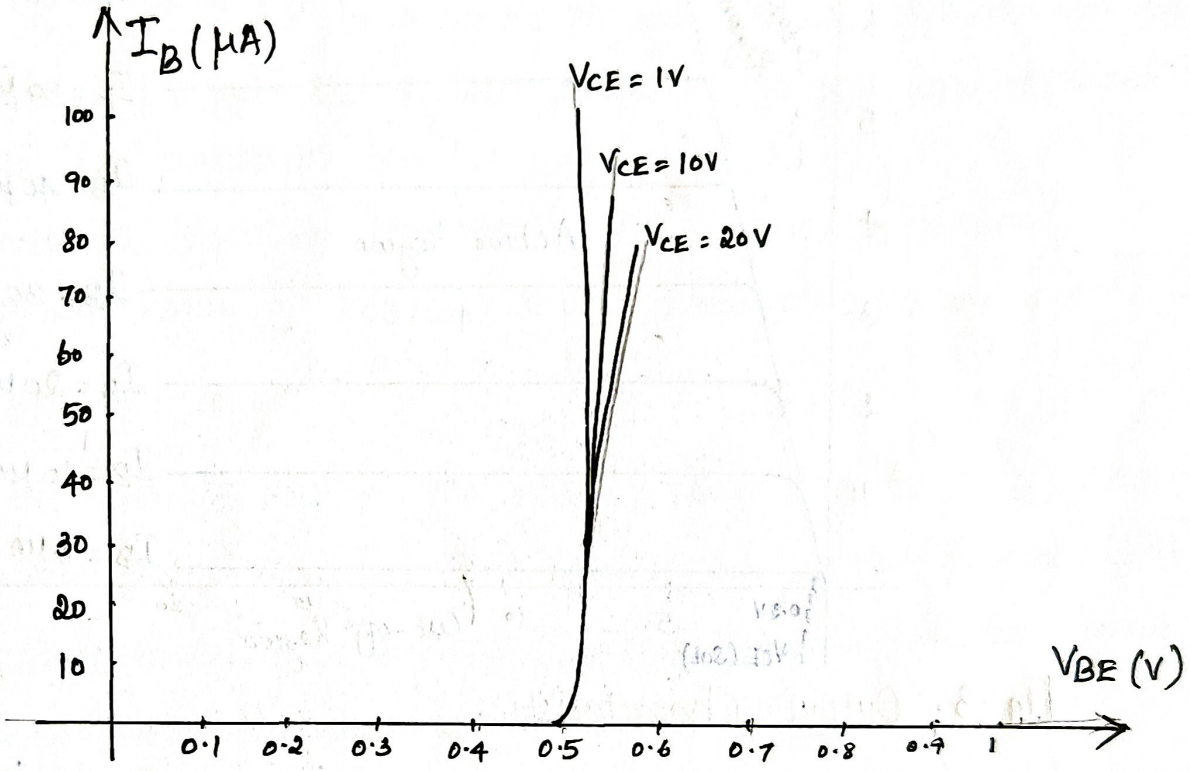


Fig. 2 Input Characteristics

DYNAMIC INPUT RESISTANCE (r_i)

i) The Input Resistance is the ratio of change in Base-Emitter Voltage (ΔV_{BE}) to the Corresponding change in Base Current (ΔI_B) at Constant Collector-Emitter Voltage (V_{CE})

$$r_i = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE}\ \text{constant}}$$

ii) There is a Slight increase in Base Current (I_B) with increase in V_{CE}

- Depletion region width at Emitter Base junction (J_E) is small because it is forward biased, whereas Depletion region width at the Collector-Base junction (J_C) is more because it is Reverse Biased.

2. OUTPUT CHARACTERISTICS

The Output Characteristics for the Common-Emitter Configuration relates an Output Current (I_C) to an Output Voltage (V_{CE}) for Various levels of Input Current (I_B) as shown in fig.3

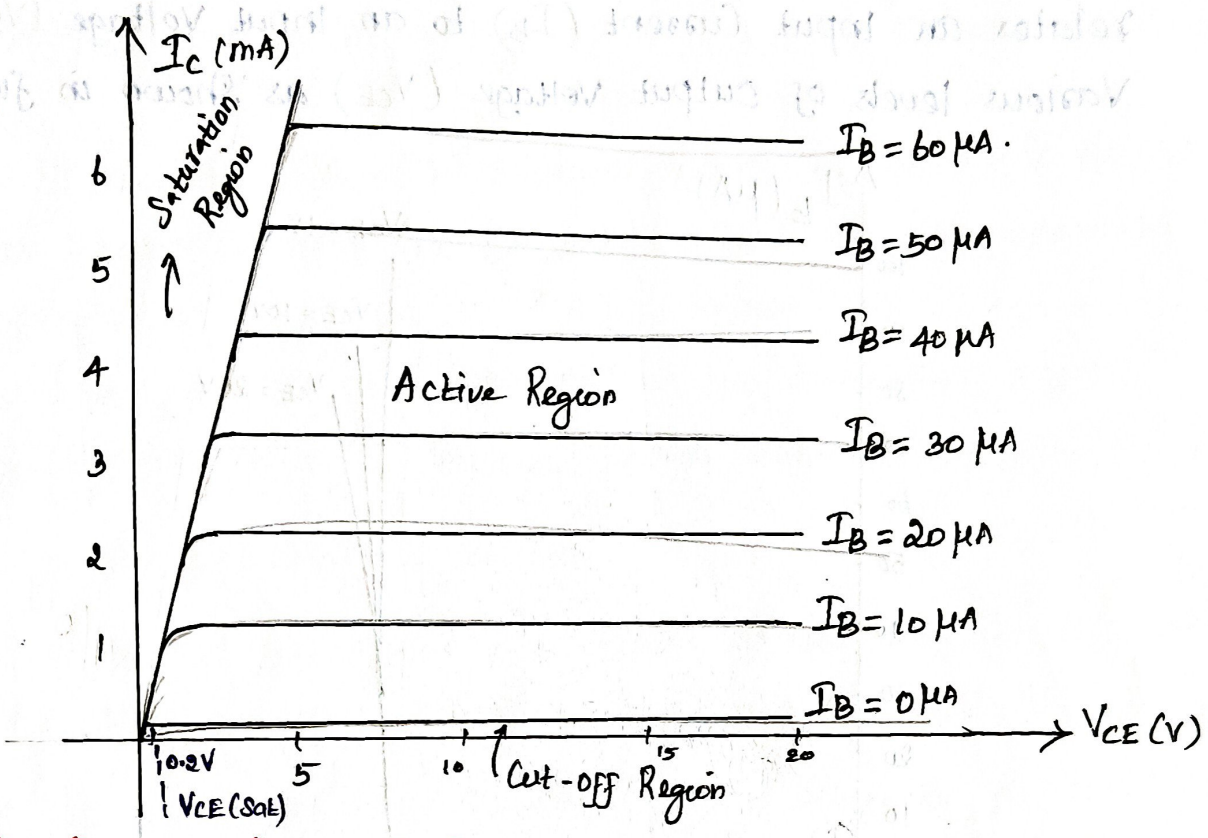


Fig.3. Output Characteristics

The Output has three basic regions of Interest i) Active Region, ii) Cut-off Region and iii) Saturation Region

i) ACTIVE REGION :

In the active Region, the Base-Emitter junction (J_E) (Emitter diode) forward biased, whereas the Collector-Base junction (J_C) (Collector diode) Reverse biased.

As V_{CE} is increased, Base Current I_B increases. Due to the Early Effect, a Very small change is reflected in a Very large change in β. $\left(\beta = \frac{\alpha}{1-\alpha}\right)$

* Hence the Output Characteristics of 'CE Configuration' show a larger slope when compared with 'CB Configuration'

ii) SATURATION REGION :

In the Saturation Region, the Base-Emitter junction (J_E) (Emitter diode) and Collector-Base junction (J_C) (collector diode) of a transistor are both 'forward-biased'

* The region to the left of $V_{CE(sat)}$ is called Saturation Region.

- If V_{CE} is reduced to a small value such as 0.2 V, the Collector diode forward biased. The Emitter diode is always forward biased to operate the transistor in 'Active Region'.

• Hence the transistor operates in the 'Saturation Region'

[The typical Value of $V_{CE(sat)}$ ranges between 0.1 V and 0.3 V]

iii) CUT-OFF REGION :

In the Cut-off Region, the Base-Emitter junction (J_E) and Collector-Base junction (J_C) of a transistor are both 'Reverse biased'.

* If the input Base Current (I_B) is Zero, the collector Current (I_C) is only due to Reverse Leakage Current (I_{CEO}). This current is Very small magnitude. The region below the Curve ($I_B = 0$) is known as the "Cut-off Region"

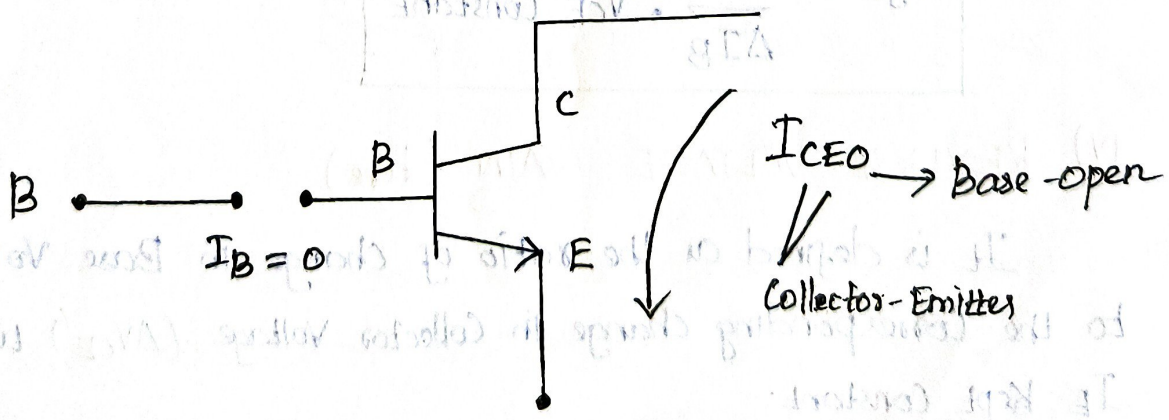


Fig.4. Reverse Leakage Current (I_{CEO})

TRANSISTOR PARAMETERS

The slope of the 'CE Characteristics' will give the following four Transistor parameters, they are commonly known as Common Emitter Hybrid Parameters or h-parameters.

i) INPUT IMPEDANCE (h_{ie})

It is defined as the ratio of change in Base Voltage (ΔV_{BE}) to the change in Base Current (ΔI_B) with the V_{CE} kept Constant.

$$h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B}, \quad V_{CE} \text{ Constant}$$

ii) OUTPUT ADMITTANCE (h_{oe})

It is defined as the ratio of change in Collector Current (ΔI_C) to the change in Collector Voltage (ΔV_{CE}) with the I_B kept Constant

$$h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}}, \quad I_B \text{ constant}$$

iii) FORWARD CURRENT GAIN (h_{fe})

It is defined as the ratio of change in Collector Current (ΔI_C) to the Change in Base Current (ΔI_B) with the V_{CE} kept Constant.

$$h_{fe} = \frac{\Delta I_C}{\Delta I_B}, \quad V_{CE} \text{ Constant}$$

iv) REVERSE VOLTAGE GAIN (h_{re})

It is defined as the ratio of change in Base Voltage (ΔV_{BE}) to the Corresponding change in Collector Voltage (ΔV_{CE}) with the I_E kept Constant.

$$h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}}, \quad I_E \text{ Constant}$$

COMMON COLLECTOR CONFIGURATION

In this Circuit arrangement, Input is applied between Base and Collector while output is taken between the Emitter and Collector.

* Here, Collector of the transistor is Common to both Input and Output Circuits and hence the name Common Collector Connection.

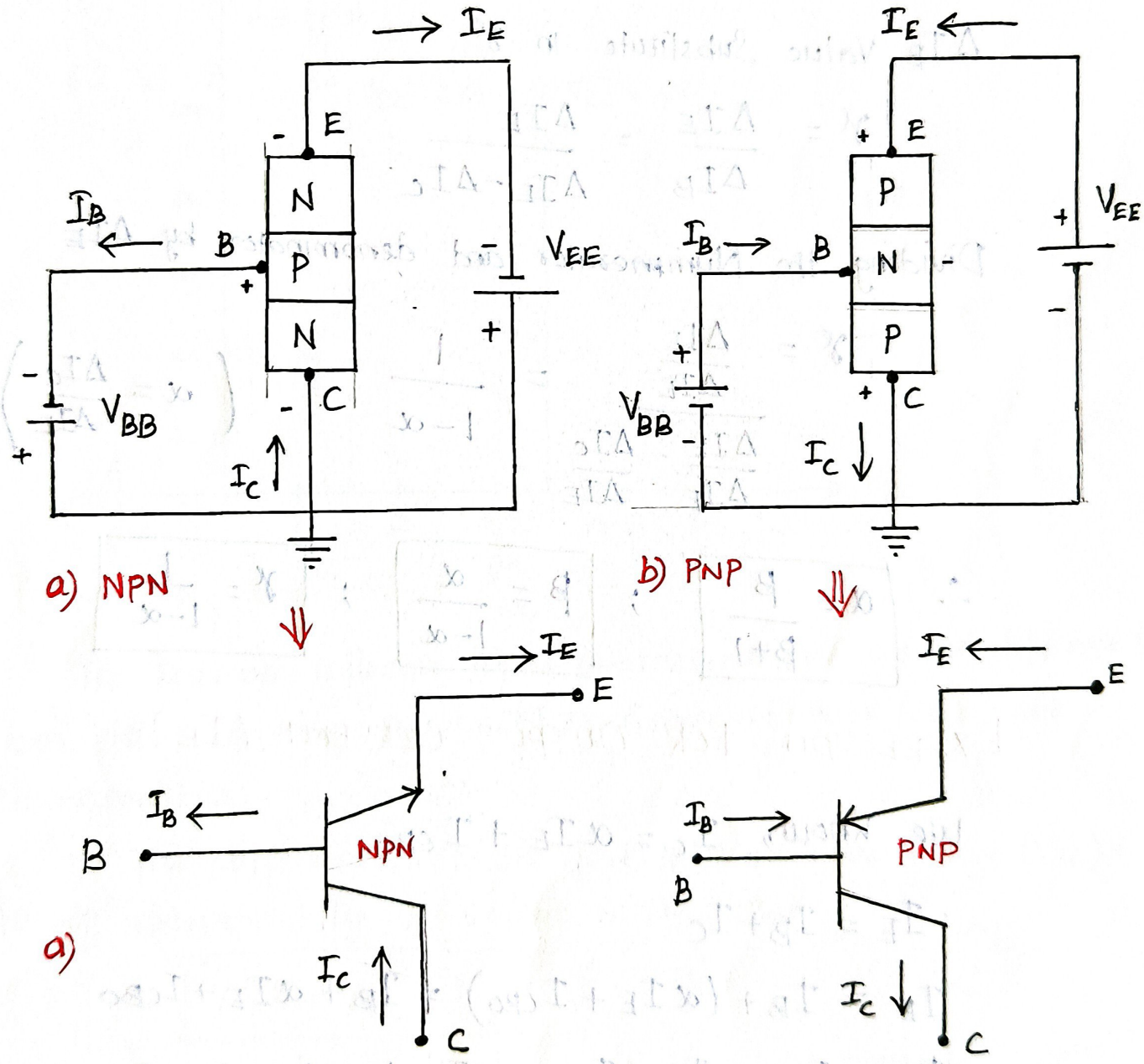


Fig-1. Notation & Symbol used with Common-Collector Configuration.

CURRENT AMPLIFICATION FACTOR (γ)

I_E is defined as the ratio of change in Emitter Current (ΔI_E) to the change in Base Current (ΔI_B) is known as Current Amplification Factor γ

$$\gamma = \Delta I_E / \Delta I_B$$

RELATION BETWEEN α, β, γ.

$$\alpha = \frac{\Delta I_C}{\Delta I_E} \; ; \; \beta = \frac{\Delta I_C}{\Delta I_B} \; ; \; \gamma = \frac{\Delta I_E}{\Delta I_B}.$$

Now, $I_E = I_B + I_C$

$$\Delta I_E = \Delta I_B + \Delta I_C$$

$$\Delta I_B = \Delta I_E - \Delta I_C$$

ΔI_B Value Substitute in γ

$$\gamma = \frac{\Delta I_E}{\Delta I_B} = \frac{\Delta I_E}{\Delta I_E - \Delta I_C}$$

Dividing the Nummerator and denominator by ΔI_E

$$\gamma = \frac{\frac{\Delta I_E}{\Delta I_E}}{\frac{\Delta I_E}{\Delta I_E} - \frac{\Delta I_C}{\Delta I_E}} = \frac{1}{1-\alpha} \qquad \left(\alpha = \frac{\Delta I_C}{\Delta I_E} \right).$$

$$\therefore \boxed{\alpha = \frac{\beta}{\beta+1}} \; ; \; \boxed{\beta = \frac{\alpha}{1-\alpha}} \; ; \; \boxed{\gamma = \frac{1}{1-\alpha}}$$

EXPRESSION FOR OUTPUT CURRENT (I_E)

We know, $I_C = \alpha I_E + I_{CBO}$

$$I_E = I_B + I_C$$

$$I_E = I_B + (\alpha I_E + I_{CBO}) = I_B + \alpha I_E + I_{CBO}$$

$$I_E - \alpha I_E = I_B + I_{CBO} \; ; \; I_E (1-\alpha) = I_B + I_{CBO}.$$

$$\boxed{I_E = \frac{I_B}{1-\alpha} + \frac{I_{CBO}}{1-\alpha}} \qquad \left(\gamma = \frac{1}{1-\alpha} \right)$$

$$\therefore \boxed{I_E = \gamma I_B + \gamma I_{CBO}}$$

COMMON COLLECTOR CHARACTERISTICS

1. INPUT CHARACTERISTICS :

The Input Characteristics for the Common-Collector Configuration is shown in figure 2 relates an Input Current (I_B) to an Input Voltage (V_{BC}) for Various levels of Output Voltage (V_{EC}) or V_{CE}

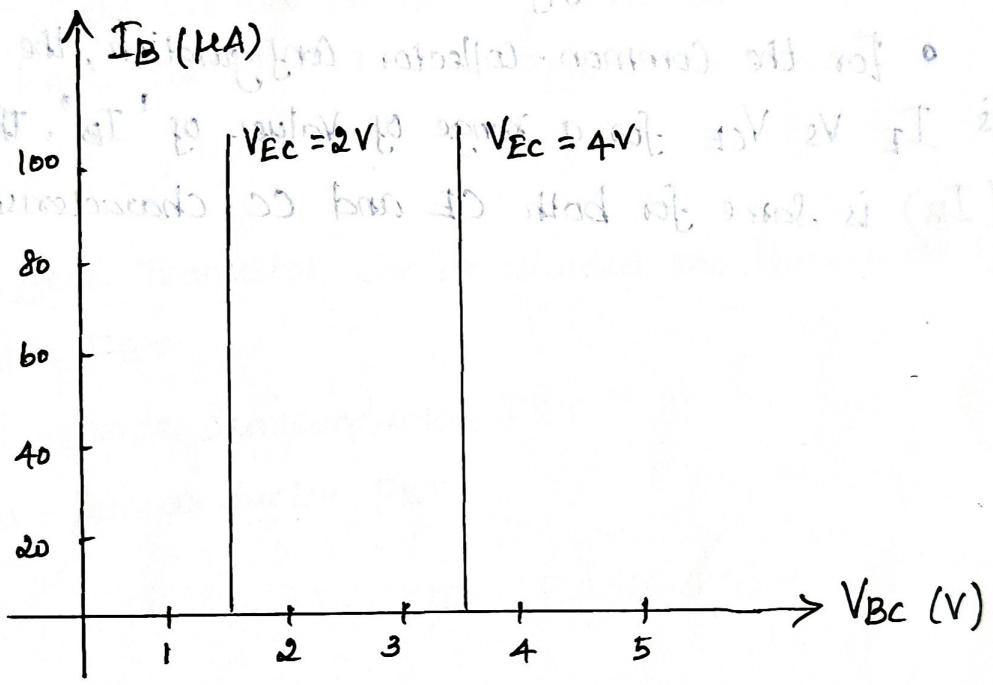


Fig. 2 . Input Characteristics .

The Common-Collector Input Characteristics (CC) are different from either Common-Base (CB) or Common-Emitter (CE) Input Characteristics.

* The difference due to the fact that the Input Voltage (V_{BC}) is largely determined by the Output Voltage (V_{CE})

$$V_{CE} = V_{BE} + V_{CB}$$



- Increasing the level of V_{CB} with V_{CE} held constant, reduces the V_{BE} and thus reduces I_B

2. OUTPUT CHARACTERISTICS

The output characteristics relates an output current (I_E) to an output voltage (V_{CE}) for various levels of input current (I_B) as shown in figure. 3.

* For all practical purposes, the output characteristics of the common-collector configuration (CC) are the same as for the common-emitter configuration (CE)

• For the common-collector configuration, the output characteristics is I_E Vs V_{CE} for a range of values of 'I_B'. The input current (I_B) is same for both CE and CC characteristics.

FIELD EFFECT TRANSISTOR (FET)

The FET is a three terminal device used for a Variety of Applications.

* The Primary difference between the two types of transistor 'BJT' is a Current-Controlled device, while the 'JFET' is a Voltage-Controlled device i.e, the Output Current is Controlled by the electric field created by the applied potential to the Control terminal. Hence the name 'Field Effect Transistor'

TYPES OF FET

Field Effect Transistor Can be divided into three main types

1. Junction FET
2. Metal-Oxide Semiconductor FET
3. Metal-Semiconductor FET

JUNCTION FIELD EFFECT TRANSISTOR (JFET)

1. CONSTRUCTION OF JFET :

A JFET is a three terminal Semiconductor device in which Current Conduction is by one type of Carrier either electrons or holes.

* The JFET Consists of a P-Type or N-type silicon Bar. The Bar is made up of N-type material which is known as 'N-Channel JFET' and if the Bar is made up of P-Type material which is known as 'P-Channel JFET'

- The Current in any FET is Carried by the 'Majority Carriers' Thus the Current is Carried by electrons in 'N-Channel JFET' and by holes in 'P-Channel JFET'

- One end of the Channel is Called the 'Source S' and the other is Called the 'Drain D'

i) SOURCE 'S' :

The Source is the terminal through which the majority Carriers enter the Bar. The Conventional Current enter the Bar at 'S' is designated by 'Is'

ii) DRAIN 'D' :

The drain 'D' is the terminal in which the majority Carriers leave the Bar. The Conventional Current enter into the Bar at 'D' is designated by 'I_D'

* The drain to Source Voltage is Called 'V_{DS}'.

iii) GATE 'G'

On both sides of the Semiconductor bar heavily doped Regions of other type impurities have been formed for creating P-N junctions.

– These impurity regions are called the 'gate G'. The Conventional Current entering the Bar at 'G' is designated by 'I_G'

CHANNEL :

The region in the Semiconductor Bar between the two gate regions through which majority carriers move from Source to drain is called the 'Channel'

2. OPERATION OF JFET :

FET works under the three conditions of

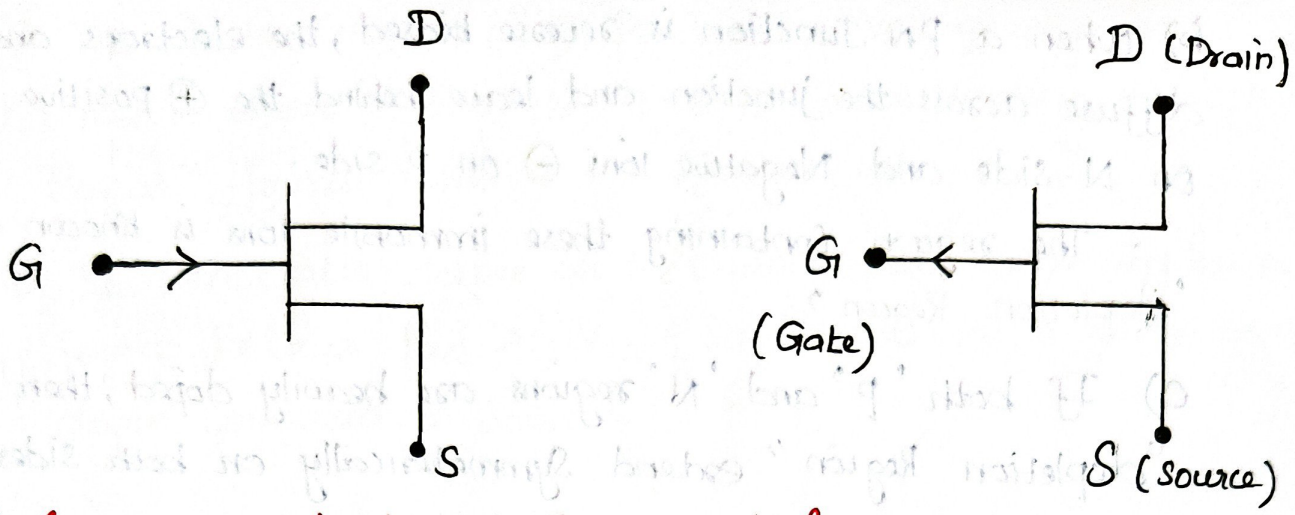
i) when V_{GG} applied and $V_{DD} = 0$

ii) when V_{DS} applied and V_{GG}

iii) when V_{DD} and V_{GG} is applied

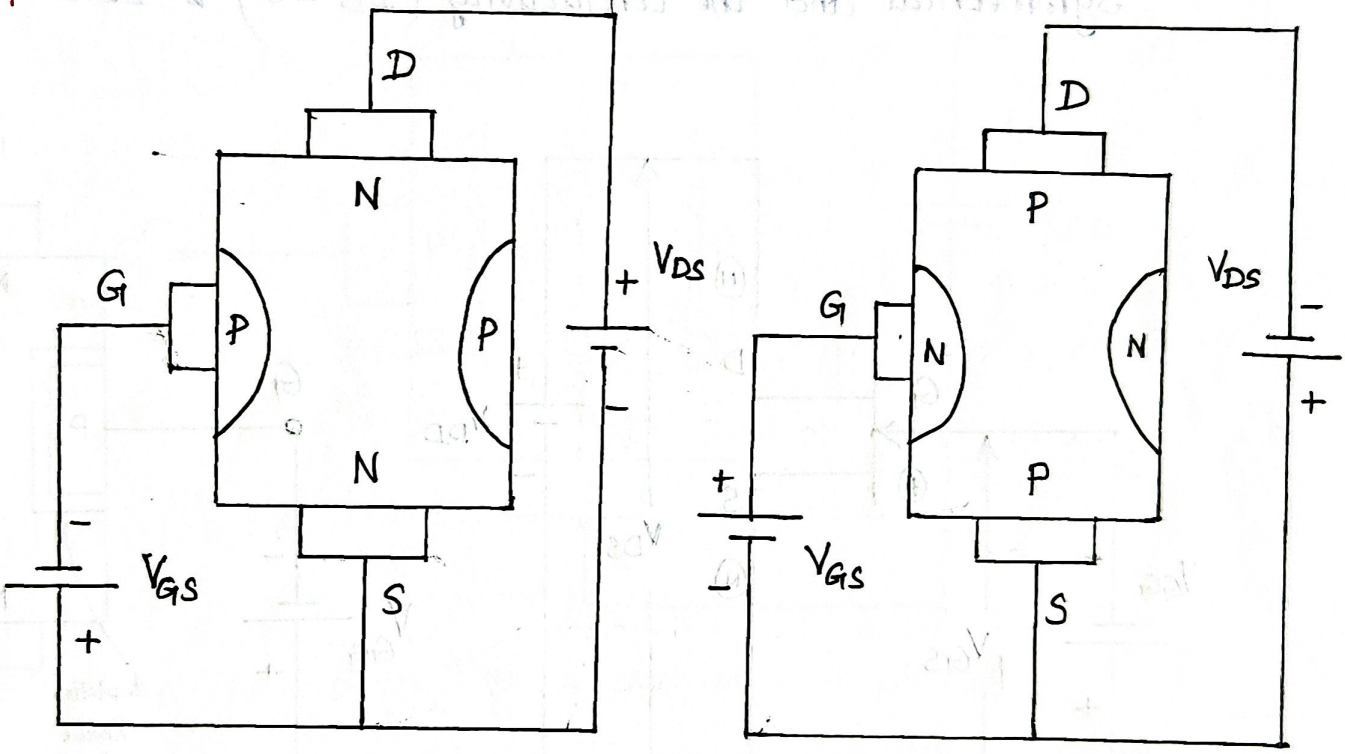
where, V_{GG} - Gate Supply Voltage ; V_{DD} - Drain Supply Voltage

$V_{DD} = V_{DS}$ - Drain Source Voltage.



a) Symbol of N-channel J-FET b) Symbol of P-channel J-FET.

Fig.1



a) Circuit diagram for N-channel JFET b) Circuit diagram of P-channel JFET.

Fig.2

i) When V_{GG} applied and $V_{DD} = 0$

Consider an N-channel JFET is shown in fig.3.

- Here, the P-type Gate and N-type channel constitute 'P-N junction'. This PN junction is always 'Reverse biased' in JFET operation.

BIASING ARRANGEMENT OF JFET:

a) The Reverse bias is applied by a Battery voltage (V_{GG}) which is connected between the Gate (G) and Source (S) terminal i.e., +ve terminal of the Battery is connected to the Source (S) and -ve terminal to the Gate (G).

b) When a PN Junction is reverse biased, the electrons and holes diffuse across the junction and leave behind the ⊕ positive ions on N-side and Negative ions ⊖ on P-side.

- The region Containing these immobile ions is known as 'depletion Region'.

c) If both 'P' and 'N' regions are heavily doped, then the "depletion Region" extend Symmetrically on both sides.

d) When no V_{DD} ($V_{DD} = 0$) is applied the depletion region is Symmetrical and the Conductivity ($I_D = 0$) is Zero.

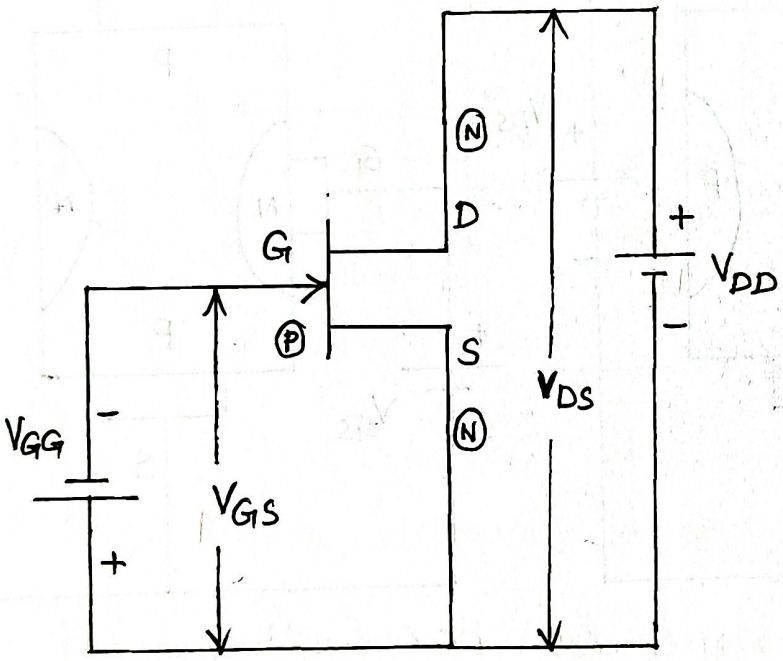


Fig.3. N-channel J-FET

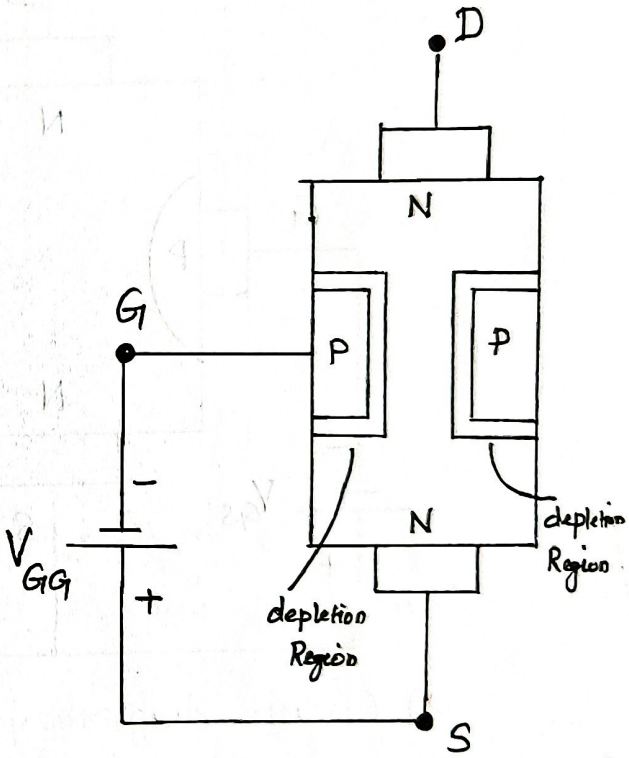


Fig.4 Circuit when V_{GG} applied.

ii) When V_{DD} is applied and $V_{GG} = 0$

a) When No Voltage is applied to Gate (G) i.e, $V_{GG} = 0$ and V_{DD} is applied between Source (S) and Drain (D)

* The electron will flow from Source (S) to Drain (D) through the channel, Constituting Drain Current (I_D).

b) The Channel Resistance are represented as 'r_d' and 'r_s' as Shown in fig.5 and its magnitude depends on "V_{DD}" and "V_{GG}"

c) The drain current (I_D) Produces a voltage drop across 'r_d' which increase biases the gate to Source junction, the "depletion Region" formed which is not Symmetrical.

d) It penetrates deeper on to channel near drain and less near Source because $V_{rd} >> V_{rs}$, So Reverse bias is higher near drain Compared to Source.

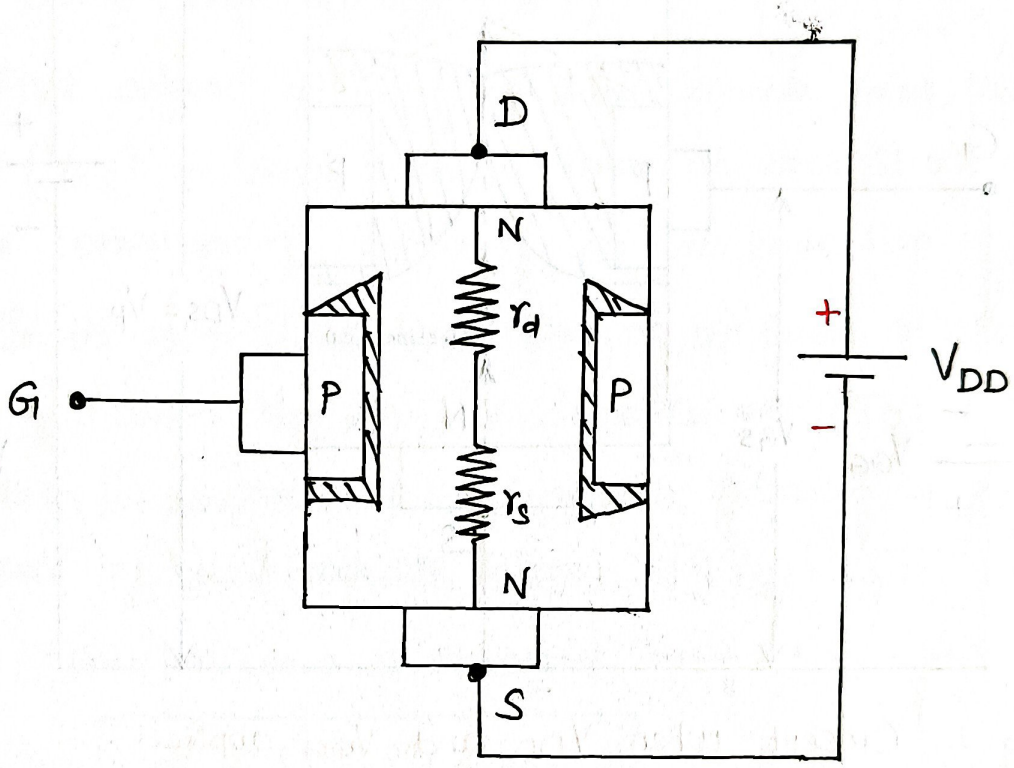


Fig.5. Circuit when V_{DD} is applied

iii) When V_{DD} and V_{GG} is applied :

(a) When Voltage is applied between the drain and Source with a battery (V_{DD}), the electrons flow from Source to drain through the narrow channel existing between the depletion Region
- This constitutes, the drain current I_D

(b) When (V_{GS}) Gate to Source Voltage is applied the input junction becomes Reverse biased, results in "depletion Region" are widened. As a result increasing Resistance of N-type Bar and Current from Source (S) to Drain (D) is decreased.

(c) When (V_{GS}) increased, further a stage is reached at which two "depletion Regions" touch each other It is called "Pinch off Region" This reduces the ($I_D = 0$) to I_D to zero.

d). If the Voltage (V_{GS}) at gate is decreased, the width of the "depletion Region" also decreases. As a result, the Current from Source (S) to Drain (D) is increased.

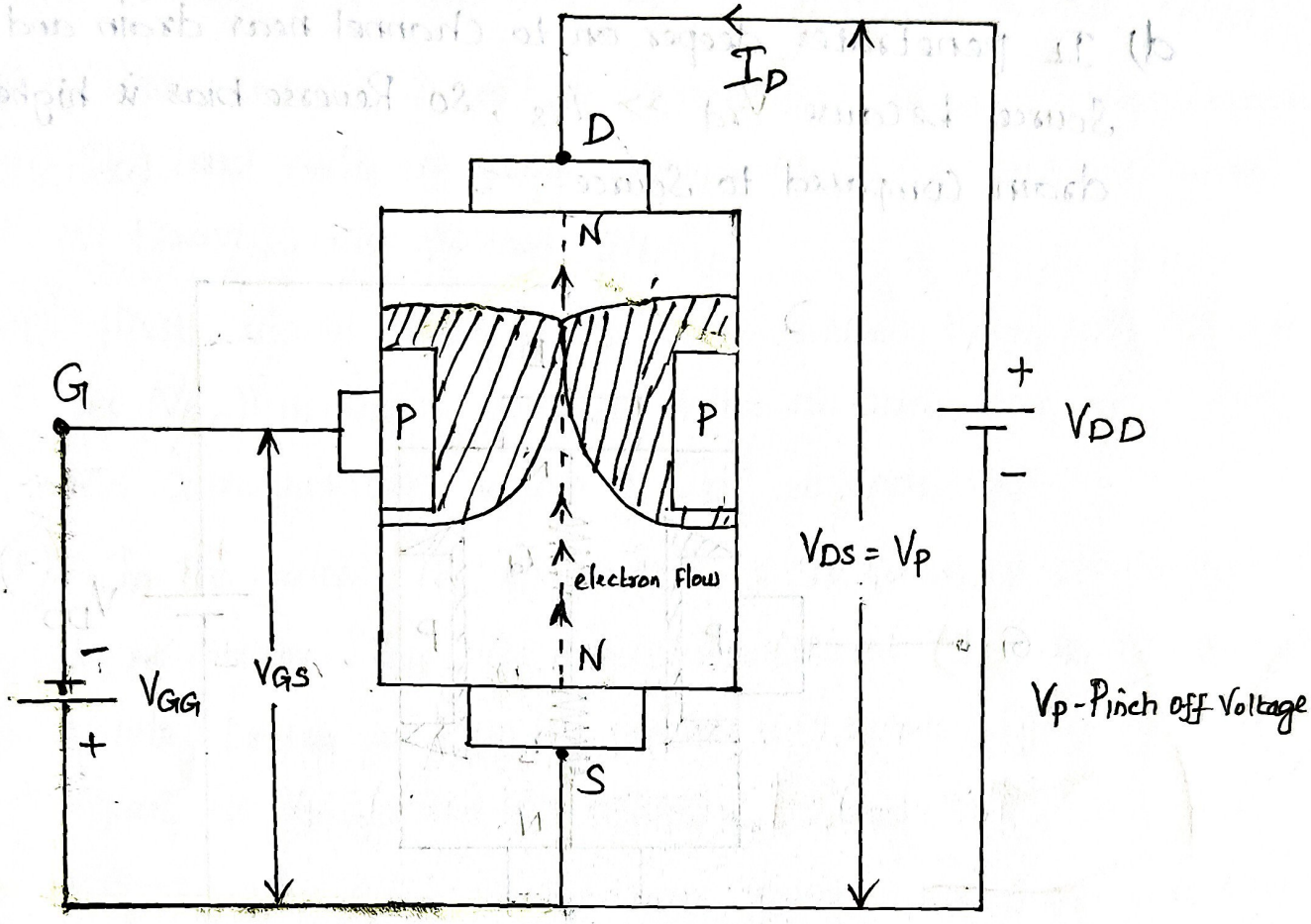


fig. 6. Circuit when V_{DD} and V_{GG} applied.

The current from Source (S) to Drain (D) can be Controlled by the Voltage on the (G). The electric field applied at the Gate (G), Controls entire operation so that the device is named as "field Effect Transistor (FET)"

CHARACTERISTICS OF JFET

We know that a family of curves that relates the Current (I) and Voltage (V) are known as "Characteristics Curve"

- There are two important characteristics of a JFET
  1. Transfer characteristics
  2. Drain characteristics.

1. TRANSFER CHARACTERISTICS :

It is drawn between Gate Source Voltage (V_{GS}) and drain Current (I_D) at Constant Drain Source Voltage (V_{DS})

(a) These Curves Shows the relationship between drain Current (I_D) and Gate to Source Voltage (V_{GS}) for different Values of Drain Source Voltage (V_{DS}).

(b) First adjust the (V_{DS}) to some Suitable Value, then Increase the (V_{GS}) in Small Suitable Value at each Step and record the Corresponding Values of 'I_D' at each Step.

(c) In the graph, the Upper end of the Curve as shown by the I_{DSS}. When $V_{GS} = 0$, the drain Current (I_D) is Maximum While Lower end of the Curve is indicated by a Voltage equal to V_p (Pinch OFF Voltage) . [$V_{GS} = V_p$]

The Transfer Curve is obtained using Shockley's Equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

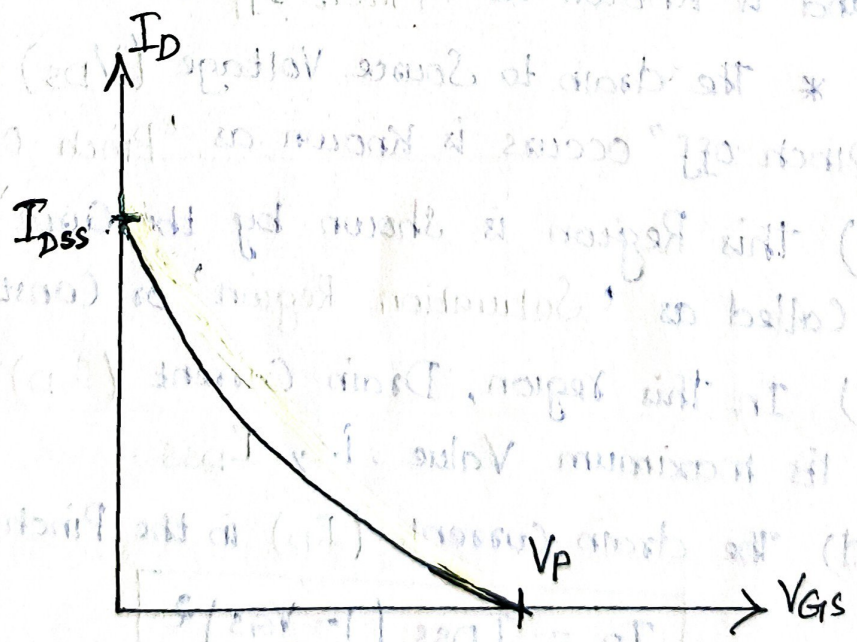


Fig.7. Transfer Characteristics.

2. DRAIN CHARACTERISTICS

Drain Characteristics shows the relation between the drain Source Voltage (V_{DS}) and Drain Current (I_D) as shown in figure. 8

i) OHOMIC REGION ($V_{GS} = 0$)

a) When $V_{DS} = 0$, there is no attracting Potential at the drain. hence drain Current $I_D = 0$.

b) As V_{DS} is Increased, the drain Current (I_D) also Increase linearly upto "Knee point" marked as 'A'

c) This shows the JFET behaves like an Ordinary Resistor Till point A is reached, this region is called as 'Ohmic Region'.

d) In this region 'AB' the drain Current (I_D) Increases at the Reverse Square law Rate, with increase in 'V_{DS}'

ii) PINCH OFF REGION

a) At the drain to Source Voltage (V_{DS}) Corresponding to point B, the channel width is reduced to a minimum Value and is known as 'Pinch Off'.

* The drain to Source Voltage (V_{DS}) at which the channel "Pinch off" occurs is known as 'Pinch Off Voltage' (V_P).

b) this Region is shown by the Curve 'BC'. It is also Called as 'Saturation Region' or Constant Current Region

c) In this region, Drain Current (I_D) remains Constant at its maximum Value, i.e, I_{DSS}.

d) The drain Current (I_D) in the Pinch off Region

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

The relation is known as "Shockley's Equation"

iii) BREAK DOWN REGION :

In this region, the drain Current (I_D) increase rapidly as the drain to Source Voltage (V_{DS}) is also increased

* It happens because of the breakdown of gate to Source junction (V_{GS}) due to "avalanche Effect". The drain to Source Voltage (V_{DS}) Corresponding to point 'C' called "Breakdown Voltage"

- The avalanche Breakdown occurs above "pinch off Region" and the drain Current (I_D) increases rapidly, as shown in fig.8

$$V_{DS}\,(\text{pinch off}) = V_p - V_{GS}$$

Where, V_p - Pinch off Voltage.

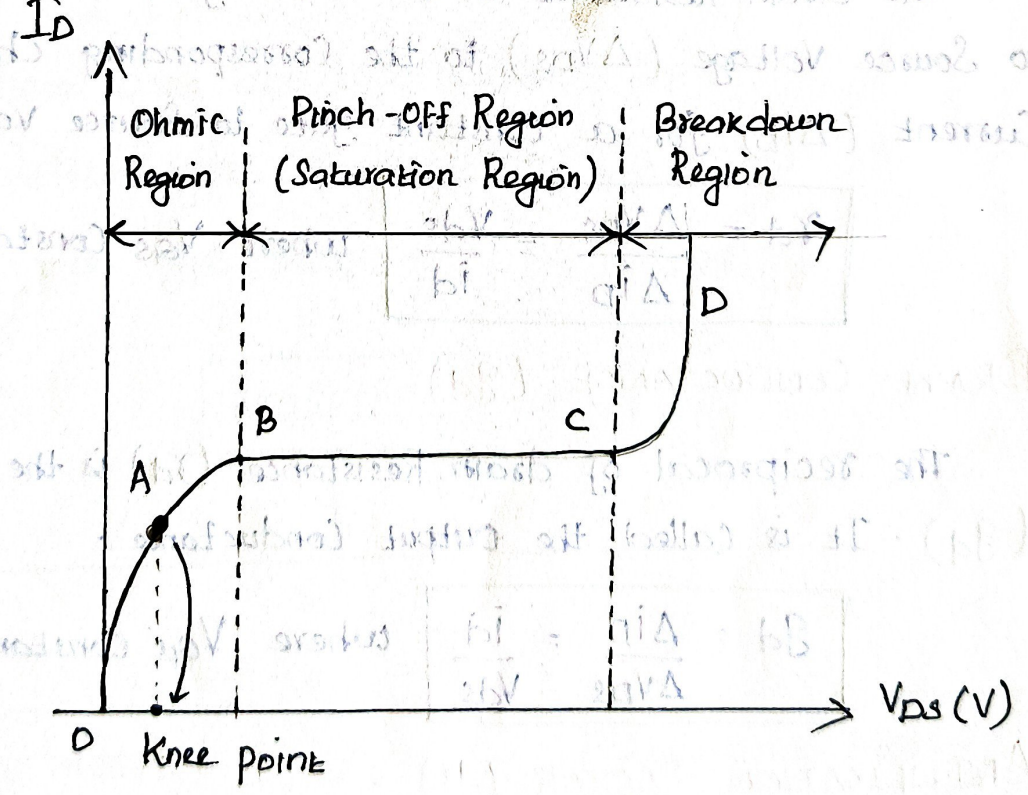


Fig.8. Drain characteristics

CHARACTERISTICS PARAMETERS OF JFET

The parameters of JFET are

i) Trans Conductance
ii) Drain Resistance
iii) Drain Conductance
iv) Amplification Factor.

i) TRANS CONDUCTANCE (g_m) [Transmittance]

The Trans Conductance is the ratio of small change in drain Current (I_D) to the corresponding change in gate to Source Voltage (V_{GS}) for a constant Drain ~~gate~~ to Source Voltage (V_{DS})

$$g_m = \frac{\Delta i_D}{\Delta V_{GS}} = \frac{i_d}{V_{gs}}$$ where V_{DS} Constant

ii) DRAIN RESISTANCE (r_d)

The drain Resistance is the Ratio of small change in drain to Source Voltage (ΔV_{DS}) to the Corresponding Change in drain Current (Δi_D) for a Constant gate to Source Voltage (V_{GS})

$$\therefore r_d = \frac{\Delta V_{DS}}{\Delta i_D} = \frac{V_{ds}}{i_d}$$ where V_{GS} Constant.

iii) DRAIN CONDUCTANCE (g_d)

The reciprocal of drain Resistance (r_d) is the drain Conductance (g_d). It is called the Output Conductance.

$$g_d = \frac{\Delta i_D}{\Delta V_{DS}} = \frac{i_d}{V_{ds}}$$ where V_{GS} Constant.

iv) AMPLIFICATION FACTOR (μ) :

It is the given by the ratio of small change in drain to Source Voltage (ΔV_{DS}) to the corresponding change in gate to Source Voltage (ΔV_{GS}) for a Constant drain Current (I_D).

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$ where I_D constant.

MOSFET - METAL OXIDE SEMICONDUCTOR FET

MOSFET is a three terminal device. The three terminals are Source (S), Gate (G), and Drain (D).

* The Gate of a MOSFET is insulated from the channel. Because of this, the MOSFET is also known as an "Insulated Gate FET" (IGFET)

i) MOSFET is a second category of Field Effect Transistor.

ii) The MOSFET differs from a JFET, it has no PN Junction Structure, instead the gate of the MOSFET is insulated from the channel by a silicon dioxide (SiO_2) layer.

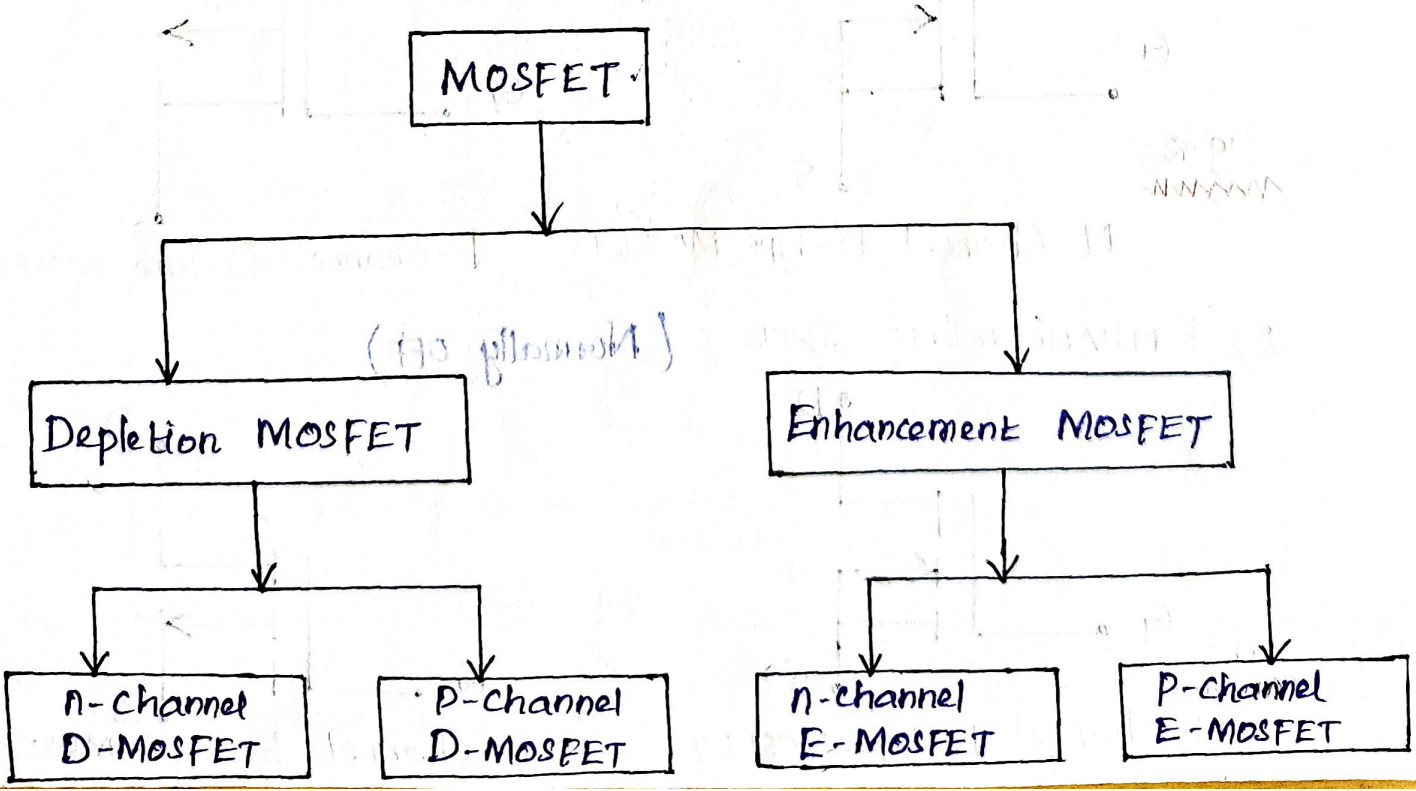
iii) Because of the insulated gate these devices are called "IGFET"

Types of MOSFET

There are two types of MOSFET.

a) Depletion type MOSFET (D-MOSFET)

b) Enhance type MOSFET (E-MOSFET)



CONSTRUCTION OF MOSFET

The Symbol and Basic construction for both configurations of MOSFET

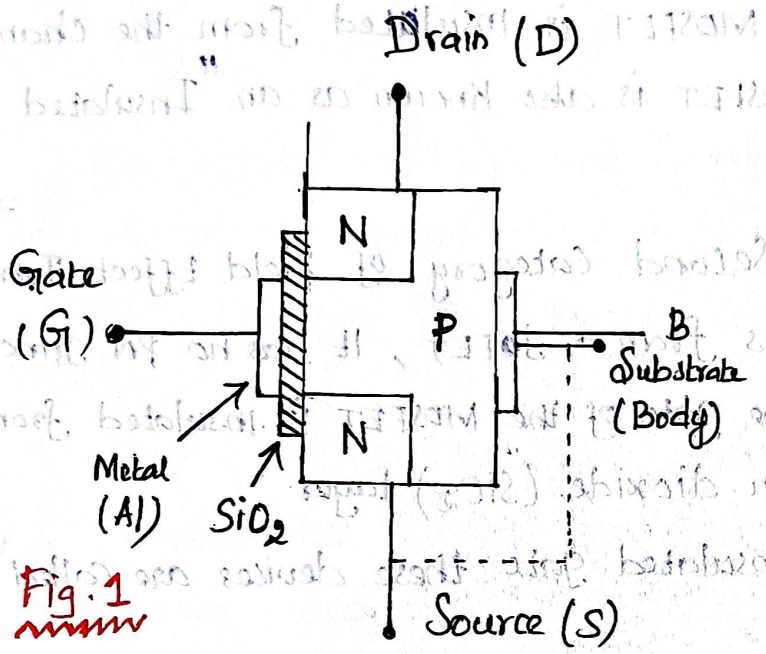
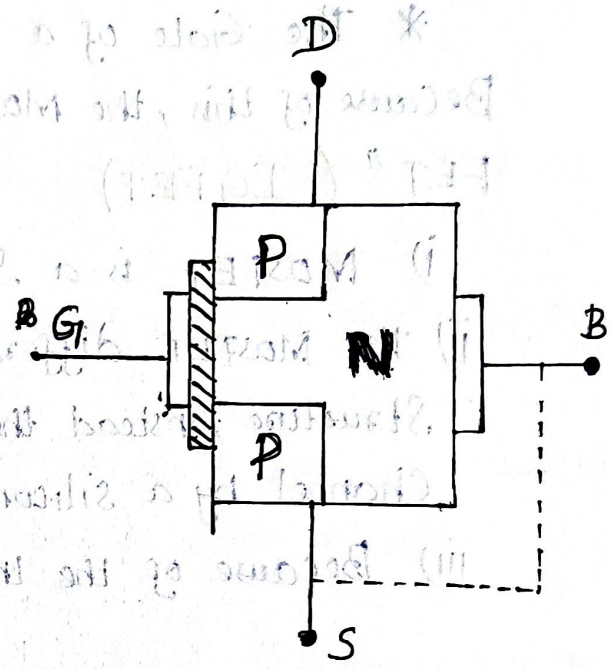


Fig. 1



N-Channel MOSFET

P-Channel MOSFET

1) DEPLETION TYPE : (Normally-ON)

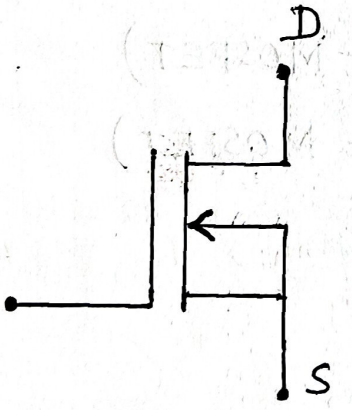
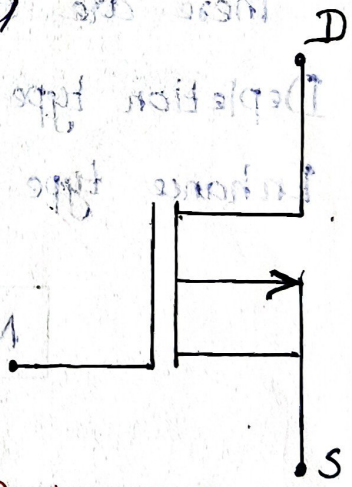


Fig. 2

N-Channel D-type MOSFET



P-channel D-type MOSFET

2) ENHANCEMENT TYPE : (Normally OFF)

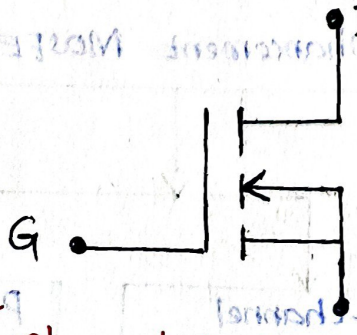
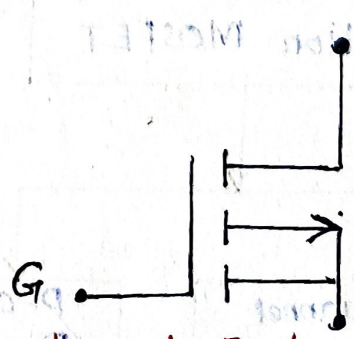


Fig. 3

N-Channel E-type MOSFET



P-Channel E-type MOSFET

DEPLETION MOSFET (D-MOSFET OR DE-MOSFET)

CONSTRUCTION OF D-MOSFET :

1. N-channel (NMOS) Depletion type MOSFET

STRUCTURE :

The basic Structure and Symbol of an N-channel depletion type MOSFET is shown in fig, 1

* It consists of a N-type material with an insulated gate for N-channel.

In N-channel (channel), the free electrons can flow from Source (S) to drain (D) through the N-type materials and P-region is called Substrate (Body or 'B')

- A thin layer of Silicon di-oxide (SiO_2) is deposited on the Channel and it is insulated with the Gate terminal (G)

* N-Channel D-MOSFET consists of a highly doped P-type Substrate. In this Substrate, two highly doped N-regions are diffused. These two regions marked as 'N' in figure

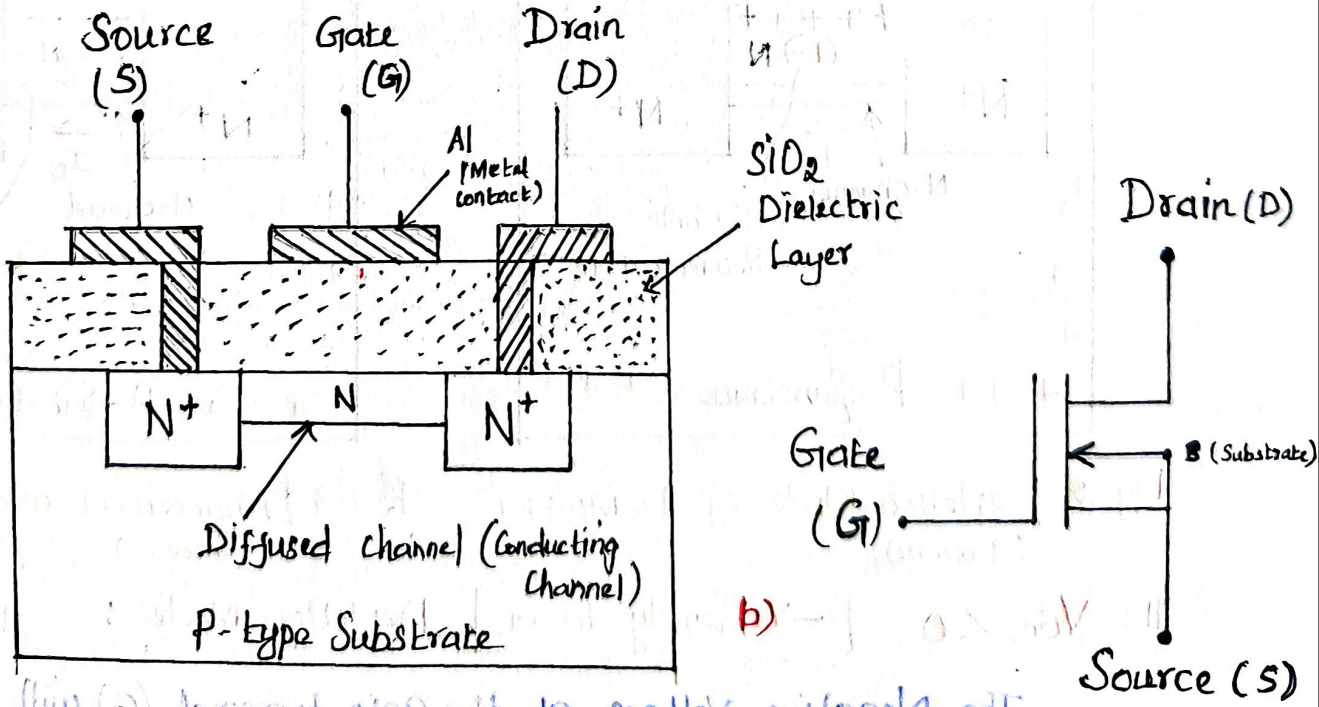


Fig.1. Structure and Symbol of n-channel Depletion type MOSFET

OPERATION OF N-CHANNEL D-MOSFET

i) $V_{GS} = 0$ and $V_{DS} > 0$.

The positive voltage is applied on the drain terminal, the (e^-) electrons in the n-channel will get attracted towards the (+) Positive terminal

– So electrons start moving from source to drain terminal and in this way current (I) starts flowing from drain (D) to source (S) in the MOSFET.

* If V_{DS} is kept increasing, then current will continue to increase until all the electrons in the channel contribute to the flow of current. After that, the current will become constant.

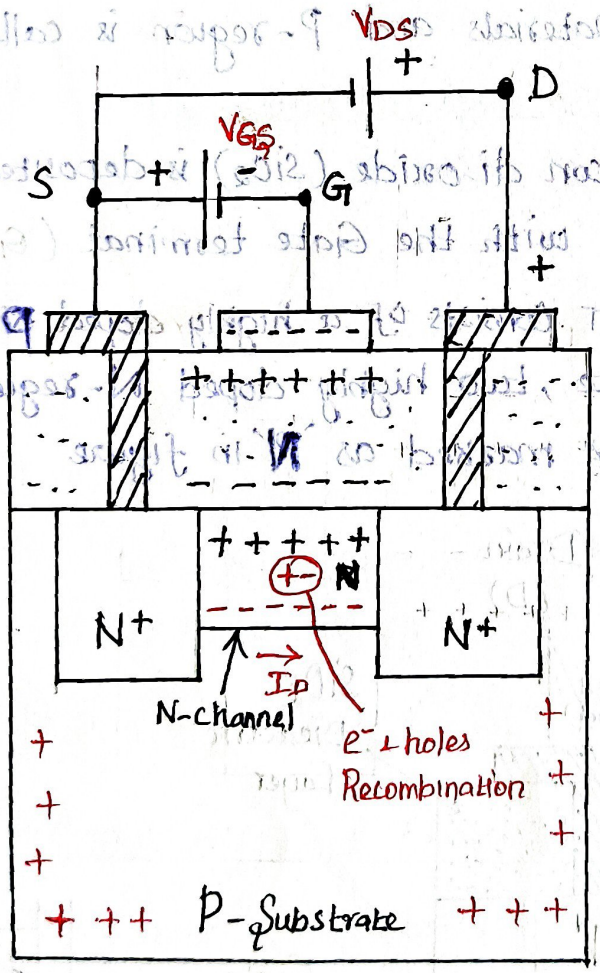


Fig. 2. Depletion Mode of D-MOSFET (Decrease)

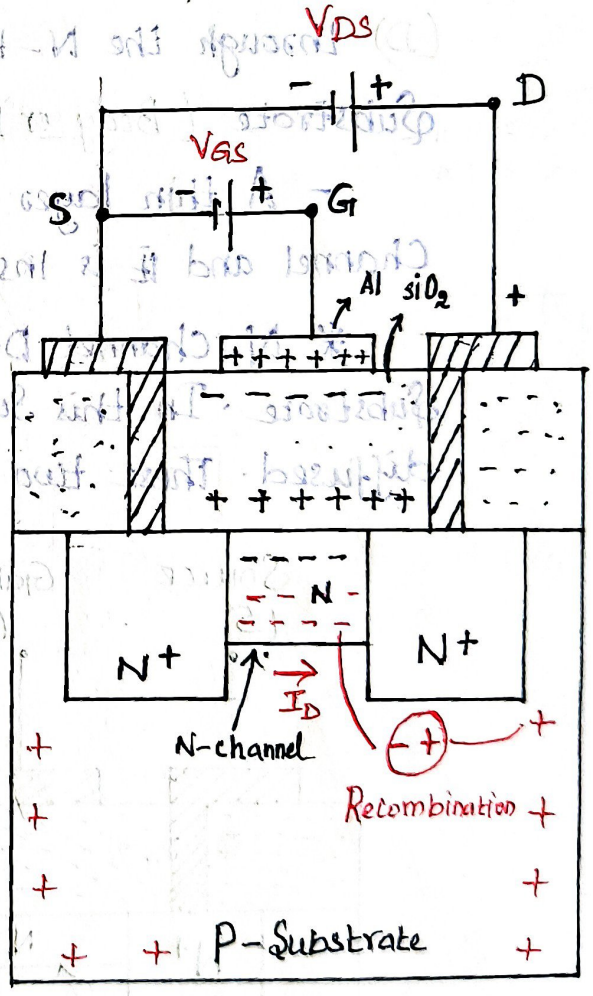


Fig. 3 Enhancement mode of D-MOSFET (Increase)

ii) $V_{GS} < 0$ [–Ve Supply to G] Depletion Mode :

The Negative Voltage at the gate terminal (G) will push electrons

towards the "P Substrate", and at the Same time '⊕ holes' in the P-type Substrate will get attracted towards the oxide layer

* Electrons ⊖ will recombine with holes ⊕ and the Number of free electrons in the "N-channel" will decrease thereby reducing the amount of Drain Current (I_D) in fig.2. [depletes the channel]

iii) $V_{GS} > 0$ [+Ve of Supply to G] Enhance Mode :

The positive Voltage at the gate terminal (G) will attract electrons towards the "p-Substrate"

* The electrons will recombine with holes and the Number of free electrons in the "N-Channel" will increase thereby Increasing the Amount of Drain Current (I_D) in fig.3. (i.e.,) 'enhance' the Conduction of the Channel

The depletion type MOSFET can be operated in two different modes as given in below :

a) DEPLETION MODE :

The device operates in this mode, when the gate voltage (V_{GS}) is Negative ⊖

b) ENHANCEMENT MODE :

The device operates in this mode, when the gate Voltage (V_{GS}) is Positive. ⊕

CHARACTERISTICS OF N-CHANNEL D-MOSFET

The different characteristics of a D-MOSFET are

a) Drain Characteristics

b) Transfer characteristics.

a) N-CHANNEL D-MOSFET DRAIN CHARACTERISTICS :

i) As the Value of V_{DS} is increased, the drain Current I_D increase and after a certain Voltage, the Current will become Constant.

ii) As the value of V_{GS} become more and more Negative ($V_{GS} < 0$) the value of drain current I_D will reduce. The voltage V_{GS} at which I_D will become zero is called 'Pinch-off voltage (V_p)'

iii) As the value of V_{GS} become positive ($V_{GS} > 0$) the value of drain current I_D will increase

iv) The curves are drawn above $V_{GS} = 0$ have positive value, the MOSFET operates in "Enhancement mode", whereas those below $V_{GS} = 0$ have Negative value and zero, the MOSFET operates in "Depletion mode"

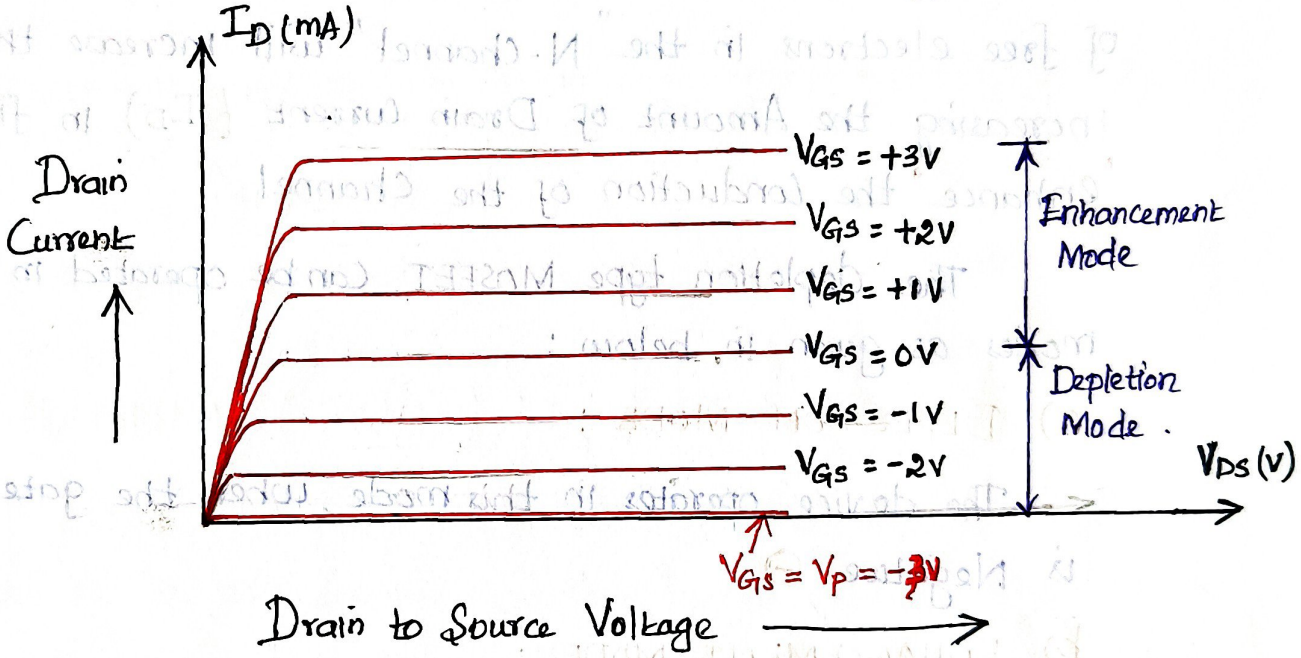


Fig. 4: Drain Characteristics of N-channel D-MOSFET

The point where $I_D = 0$ corresponds to V_p ($V_{GS\,OFF}$).

The drain current I_D at any instant is given by

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(OFF)}}\right]^2$$

b) N-CHANNEL D-MOSFET TRANSFER CHARACTERISTICS

The transfer characteristics are also called as 'transconductance curve'.

* The value I_{DSS} denotes the current from drain to source with $V_{GS} = 0$.

The depletion MOSFET (D-MOSFET) can operate with either positive or negative gate voltages. This is indicated on the transfer characteristics curves in the fig.5.

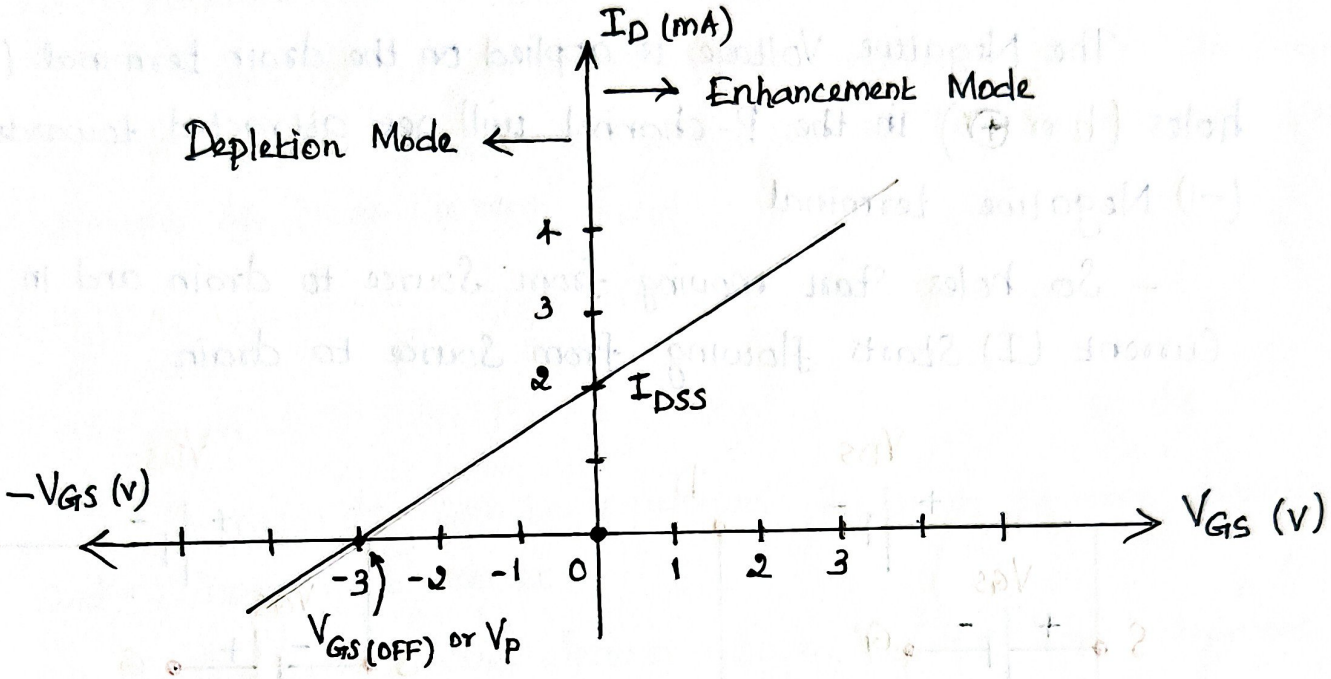


Fig.5. Transfer characteristics of N-Channel D-MOSFET

2. P-CHANNEL (PMOS) DEPLETION MOSFET

P-channel D-MOSFET consist of a highly doped N-type substrate. In this substrate, two highly doped P-regions are diffused. These two regions marked as 'P' in figure.1

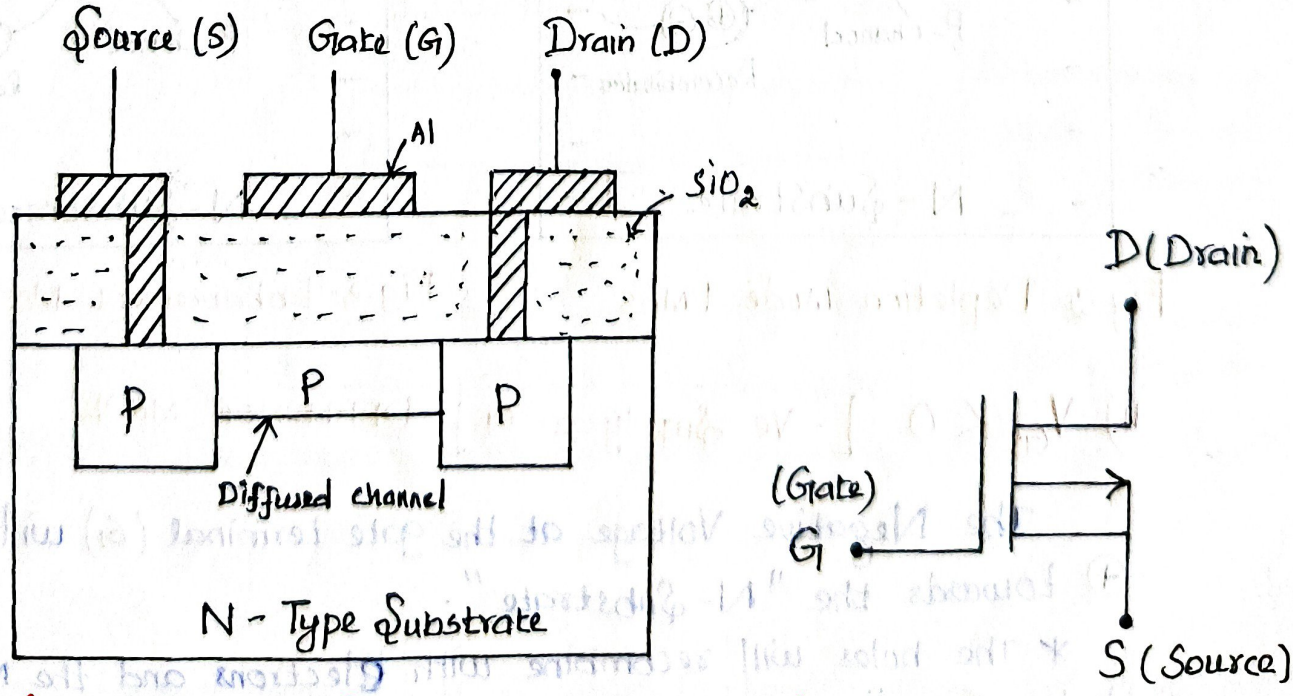


Fig.1 Structure and symbol of P-channel D-MOSFET.

OPERATION OF P-CHANNEL D-MOSFET

i) $V_{GS} = 0$ and $V_{DS} < 0$

The Negative Voltage is applied on the drain terminal (D), the holes (h or ⊕) in the P-channel will get attracted towards the (−) Negative terminal

– So holes start moving from Source to drain and in this way Current (I) starts flowing from Source to drain

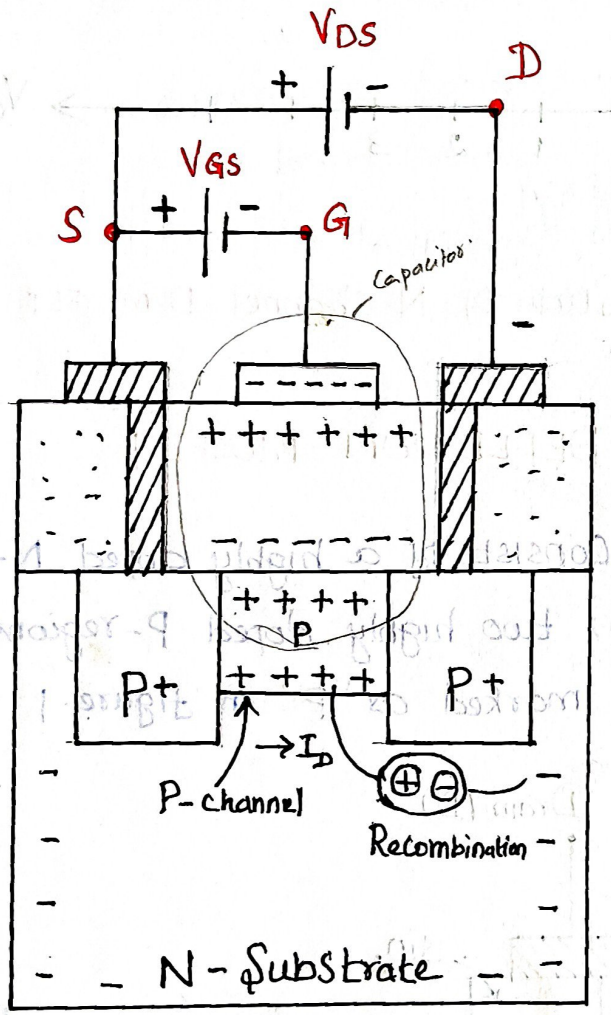


Fig.2 Depletion Mode PMOS

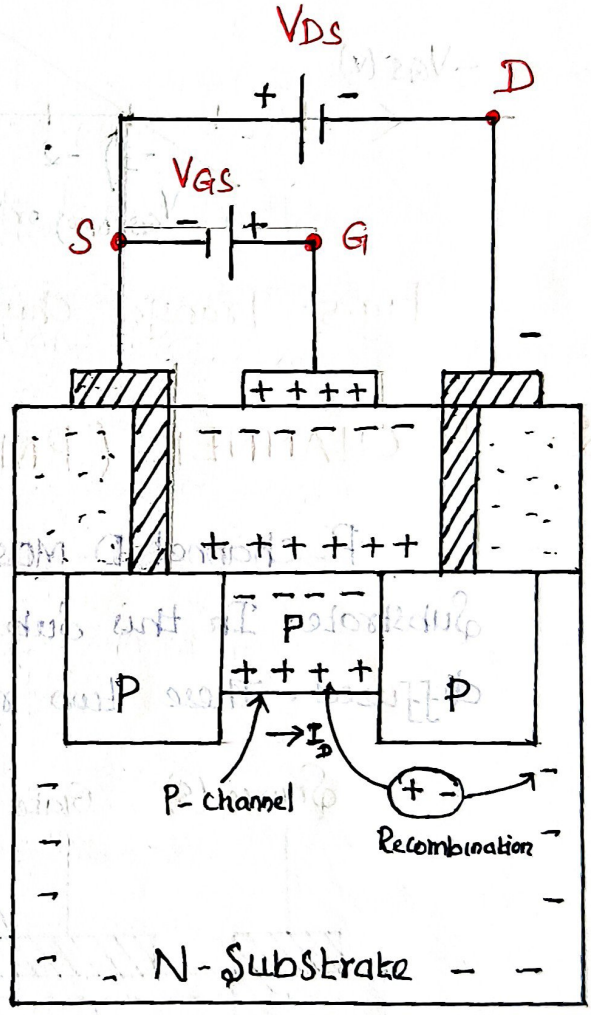


Fig.3. Enhancement Mode PMOS

ii) $V_{GS} < 0$ [−Ve Supply to G] DEPLETION MODE

The Negative Voltage at the gate terminal (G) will attract holes ⊕ towards the "N-Substrate".

* The holes will recombine with electrons and the Number of holes in the "P-channel" will increase thereby increasing I_D

iii) $V_{GS} > 0$ [+Ve of Supply to G] ENHANCEMENT MODE :

The positive Voltage at the gate terminal (G) will pushed holes towards the "N-Substrate"

* Holes ⊕ will recombine with electrons ⊖ and the Number of holes in the "p-channel" will decrease thereby reducing the amount of Drain Current I_D

CHARACTERISTICS OF P-CHANNEL D-MOSFET

a) P-CHANNEL D-MOSFET DRAIN CHARACTERISTICS :

D-MOSFET can be operated for both ~~positive~~ depletion and Enhancement modes.

* The curves are drawn above $V_{GS} = 0$ have Negative Value, the MOSFET operates in "Enhancement mode" whereas those below $V_{GS} = 0$ have positive Value, the MOSFET operates in "Depletion mode"

– It is exactly similar to N-channel except that the Voltage and Current directions would be reversed.

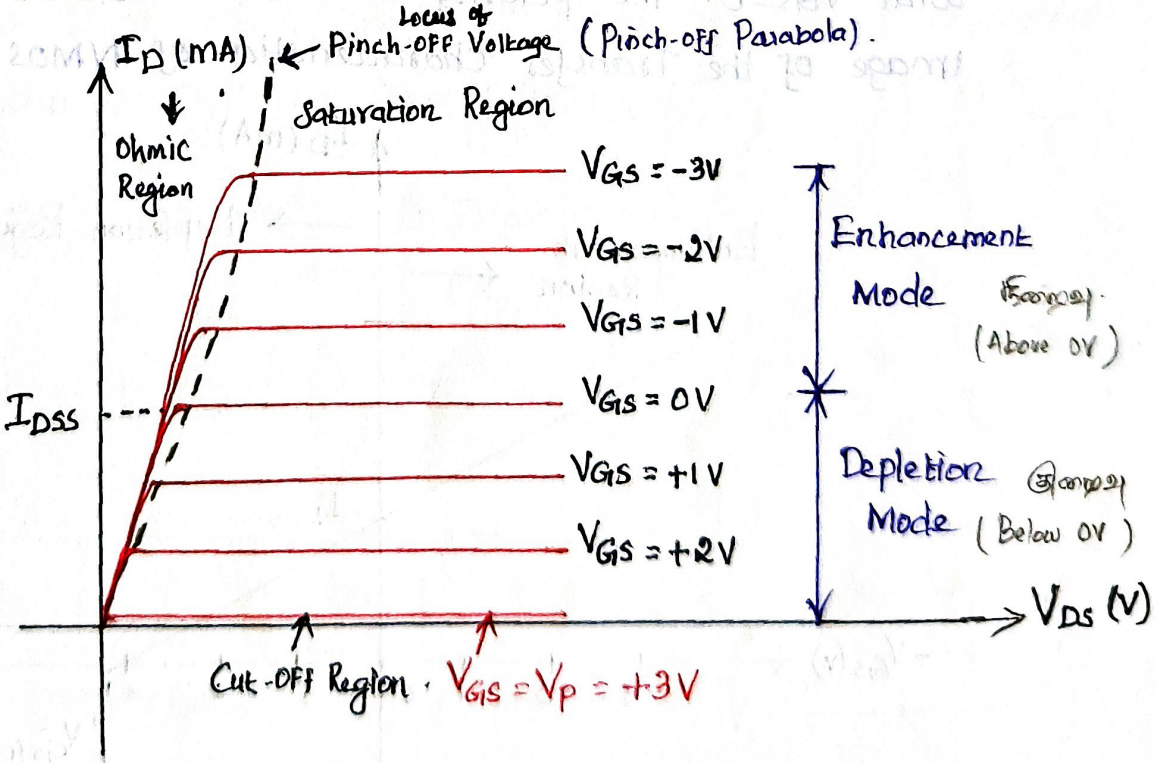


Fig. 4. Drain characteristics of p-channel MOSFET.

The I_D increases from 'Cut-OFF' in ~~Positive~~ Positive V_{GS} region (depletion mode) to I_{DSS}. and then rises for more and more Negative Values of V_{GS} (Enhancement mode)

i) CUT-OFF REGION :

In this region, No current ($I=0$) flows through it and the MOSFET is OFF

ii) OHMIC REGION :

In this region, response is linear in the curve. When the drain to Source Voltage (V_{DS}) increases, drain Current (I_D) also increases. Used as amplifier in this region

iii) Saturation Region :

Drain Current (I_D) is constant for drain Source Voltage (V_{DS}). Used as 'Switch' in this region. This occurs when the drain Source Voltage reaches 'Pinch-off Voltage (V_P)'

b) P-CHANNEL D-MOSFET TRANSFER CHARACTERISTICS :

The transfer characteristics are also called as 'Transconductance' Curve

- The Value I_{DSS} denotes the current from drain to Source with $V_{GS}=0$. The polarity inversion in V_{GS} ends in a Mirror image of the Transfer characteristics of NMOS

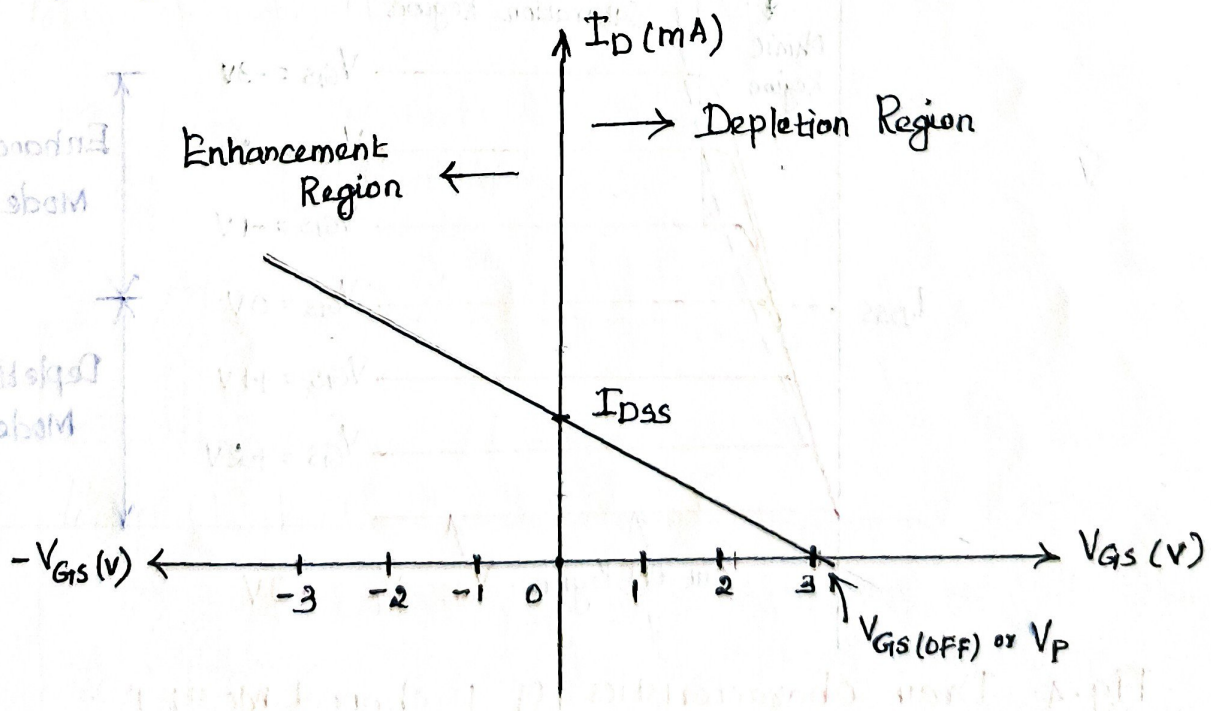


Fig.5. Transfer characteristics of P-channel D-MOSFET :

ENHANCEMENT MOSFET (E-MOSFET)

PRINCIPLE :

By applying a transverse Electric field across an insulator, deposited on the semiconductor material, thickness and hence the Resistance of a Conducting Channel of a semiconductor material can be controlled.

i) In a D-MOSFET, the Controlling the electric field reduces the Number of majority Carriers available for Conduction.

ii) In a E-MOSFET, application of electric field Causes an Increase in the Majority Carriers in the Conducting Regions

1. N- CHANNEL ENHANCEMENT (NMOS E-MOSFET)

CONSTRUCTION :

As there is no Continuous Channel in an E-MOSFET, this Condition is represented by the broken line in the symbols.

* The Construction and the Circuit symbol of N-channel Enhancement MOSFET are shown in fig. 1.

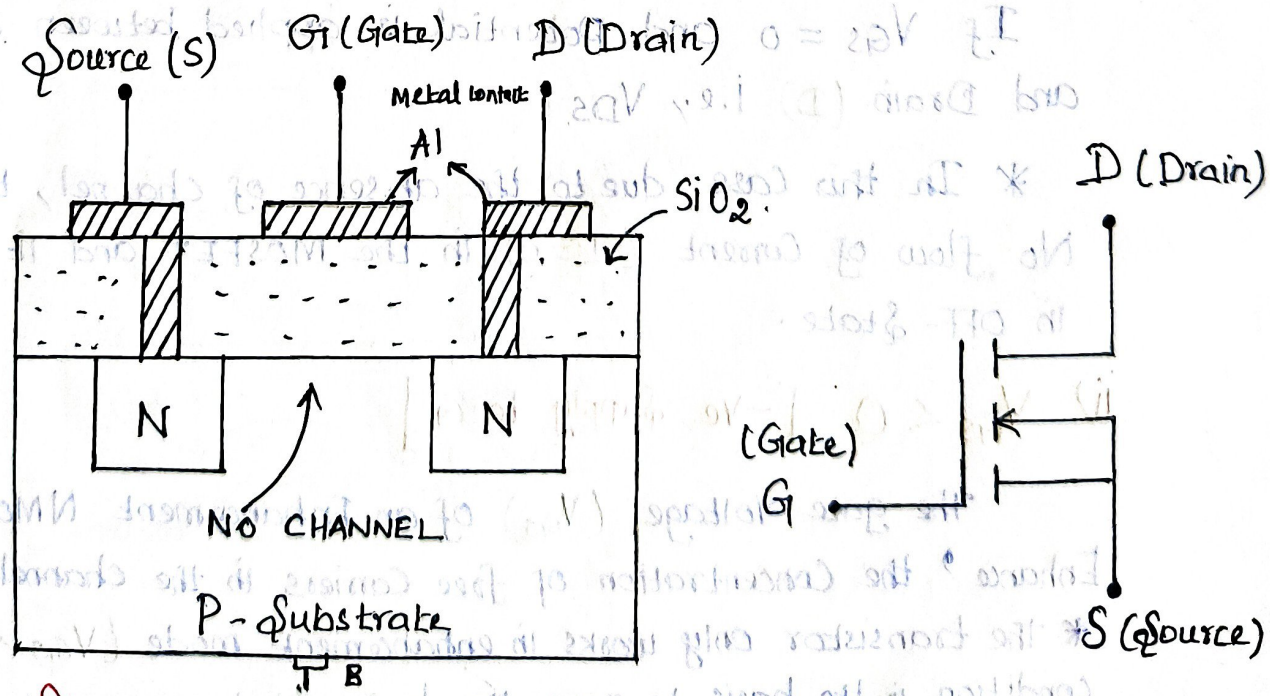


Fig. 1 Structure and Symbol of N-channel E-MOSFET.

i) Two highly doped N^+ regions are diffused in a Lightly doped Substrate of "P-Type Silicon Substrate". One N+ region is called the Source (S) and the other one is called the Drain (D)

ii) They are Separated by 1 mil (10^{-3} inch). A thin Insulating layer of SiO_2 is grown over the Surface of the Structure and holes (h) are cut into the oxide layer, allowing Contact with Source and Drain.

iii) Then a thin layer of Metal Aluminium (Al) is formed over the layer of SiO_2. This metal layer Covers the entire channel Region and it forms the Gate (G).

iv) The metal Area of the Gate, in Conjunction with the insulating Oxide layer of SiO_2 and the Semiconductor channel forms a 'Parallel Plate Capacitor'.

v) This device is called the Insulated Gate FET (IGFET) because of the insulating layer of SiO_2. This layer gives an extremely high input impedance for the MOSFET

OPERATION OF N-CHANNEL E-MOSFET

i) $V_{GS} = 0$ and $V_{DS} > 0$

If $V_{GS} = 0$ and potential is applied between Source (S) and Drain (D) i.e., V_{DS}

* In this case, due to the absence of channel, there will be No flow of Current ($I = 0$) in the MOSFET and it will remain in OFF-State.

ii) $V_{GS} < 0$ [-ve Supply to G]

The gate Voltage (V_{GS}) of an Enhancement NMOS Can 'Only Enhance' the Concentration of free Carriers in the channel.

* the transistor only works in enhancement mode ($V_{GS} > 0$). This condition is the basis to name the device 'Enhancement Mode MOSFET'

iii) $V_{GS} > 0$ [+ve Supply to Gate] ENHANCEMENT MODE

If the P-Substrate is grounded and a positive Voltage is applied at the Gate (G), the positive charge ⊕ on G induces an equal Negative charge ⊖ on the P-Substrate side between the Source and Drain Regions

* The direction of the electric field is perpendicular to the 'plates of the Capacitor' through the Oxide (SiO_2 layer)

- The Negative charge of electrons (e^-) which are Minority Carriers in the 'P-Type Substrate' forms an 'Inversion Layer'

* Now this Inversion Layer will act as a channel between Source and Drain. Thus a channel is Created between drain and Source.

- As the positive Voltage on the gate (V_{GS}) Increases, the 'Induced Negative charge' in the Semiconductor Increase. Hence the Conductivity Increases and Current (I) flows from Source to Drain. Thus the drain Current (I_D) is enhanced (Increase) by the positive Voltage as shown in fig. 2.

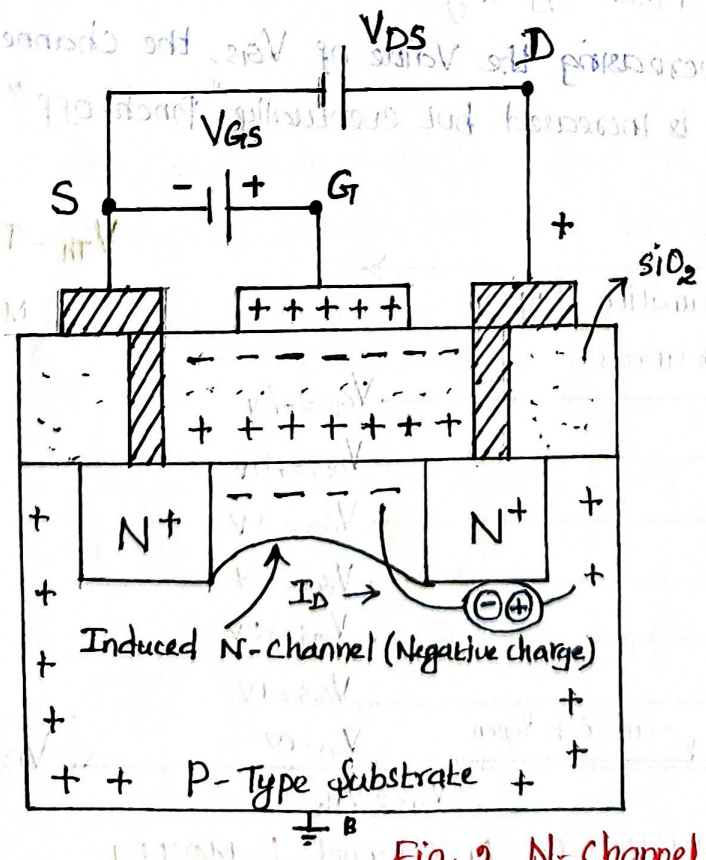


Fig. 2. N-Channel E-MOSFET

iv) $V_{GS} > 0$ and $V_{DS} > 0$

In this case, Current (I) can flow through the channel. The Value of V_{GS} at which the "Inversion Layer" is formed is called "Threshold Voltage (V_{th})".

* Below this Voltage, No current (I=0) flows through MOSFET.

CHARACTERISTICS OF N-CHANNEL E-MOSFET

a) N-CHANNEL E-MOSFET DRAIN CHARACTERISTICS :

* This curve is a plot of drain current (I_D) and V_{DS} at different V_{GS}. As the Value of V_{GS} is increased, the drain current I_D is also increased.

i) When $V_{GS} < V_{Th}$ the line is very close to the axis because the Current through MOSFET is almost Zero ($I = 0$) i.e., "Cut-off region"

ii) When $V_{GS} > V_{Th}$, the current starts to increase and Ultimately there comes a point i.e., "Ohmic Region" and when 'Pinch-off' (V_p) occurs and the Current becomes Constant i.e., "Saturation Region or Pinch off Region"

iii) If we keep increasing the Value of V_{GS}, the channel get wider that means the I_D is increased but eventually "Pinch-off" occurs.

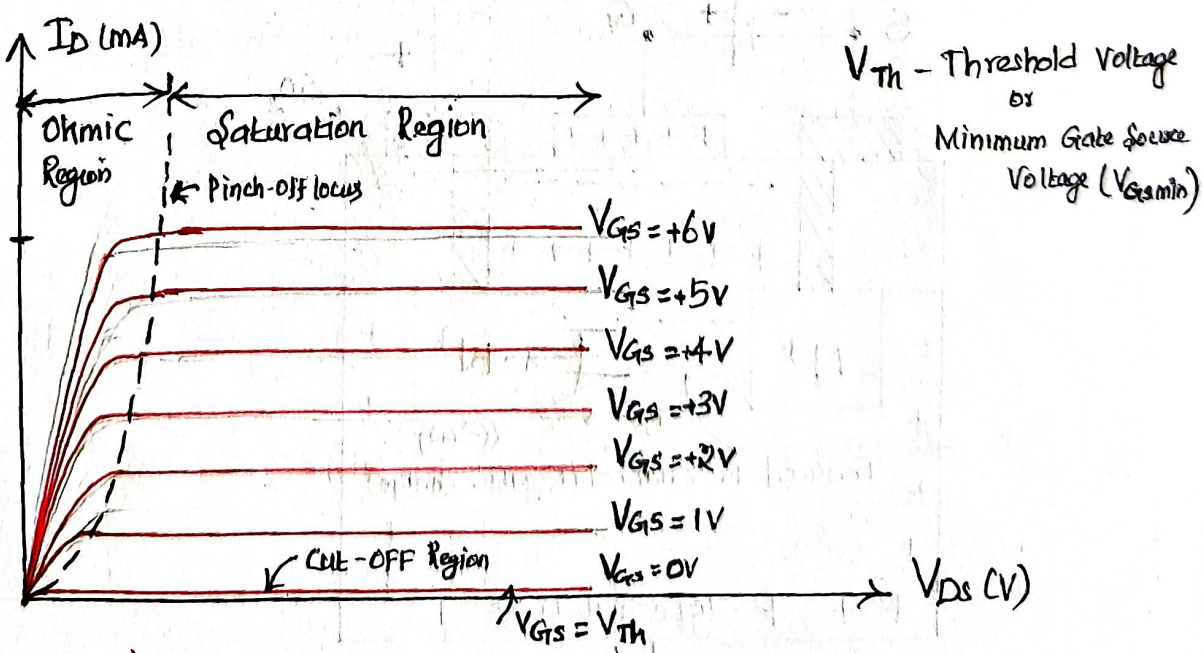


Fig.3. Drain Characteristics of N-channel E-MOSFET

b) N-CHANNEL E-MOSFET TRANSFER CHARACTERISTICS

The transfer characteristics show the relationship between the input voltage V_{GS} and output current I_D at constant 'V_{DS}'

* Below threshold V_{Th}, the drain current ($I_D = 0$) is zero. Above threshold V_{Th}, the drain current I_D increases with an increase in the V_{GS}.

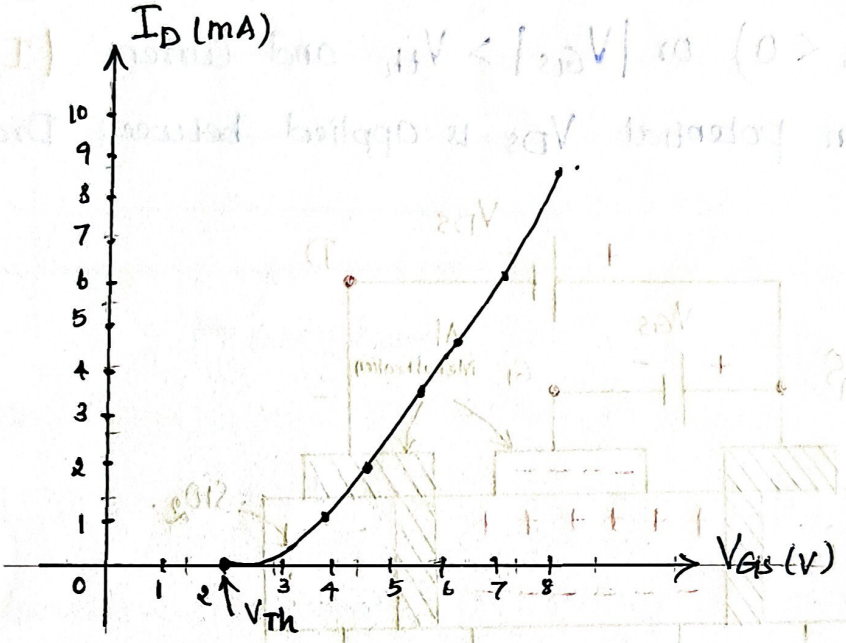


Fig. 4. Transfer characteristics of N-channel E-MOSFET.

2. P-CHANNEL (P-MOS) ENHANCEMENT TYPE MOSFET

STRUCTURE :

There are two heavily doped P-Regions known as Source (S) and Drain (D) doped into the "N-Type Substrate".

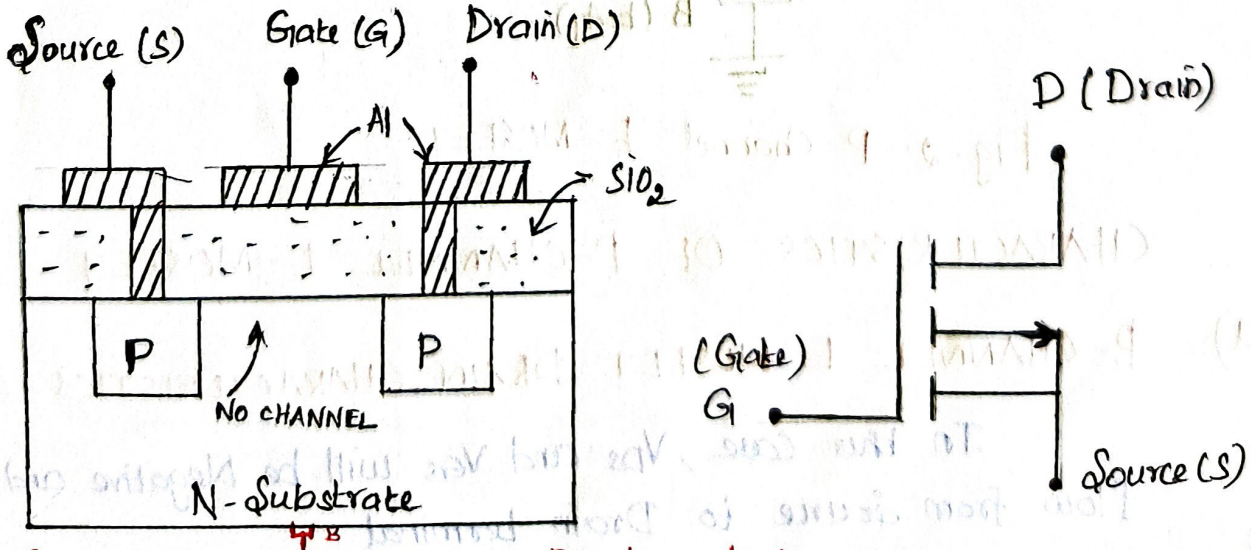


Fig. 1. Structure and symbol of P-channel E-MOSFET.

OPERATION OF P-CHANNEL E-MOSFET.

The operation is very similar to the 'N-Channel E-MOSFET' except in this case, polarity of voltages and direction of flow of current will be Reversed.

i) Now the 'P-Channel' will be formed (Induced P-channel or Positive charge) when the applied voltage V_{GS} is Negative ($V_{GS} < 0$) or $|V_{GS}| \geq V_{th}$ and current (I) starts flowing when potential V_{DS} is applied between Drain and Source. (Ohmic ~~Saturation~~ Region)

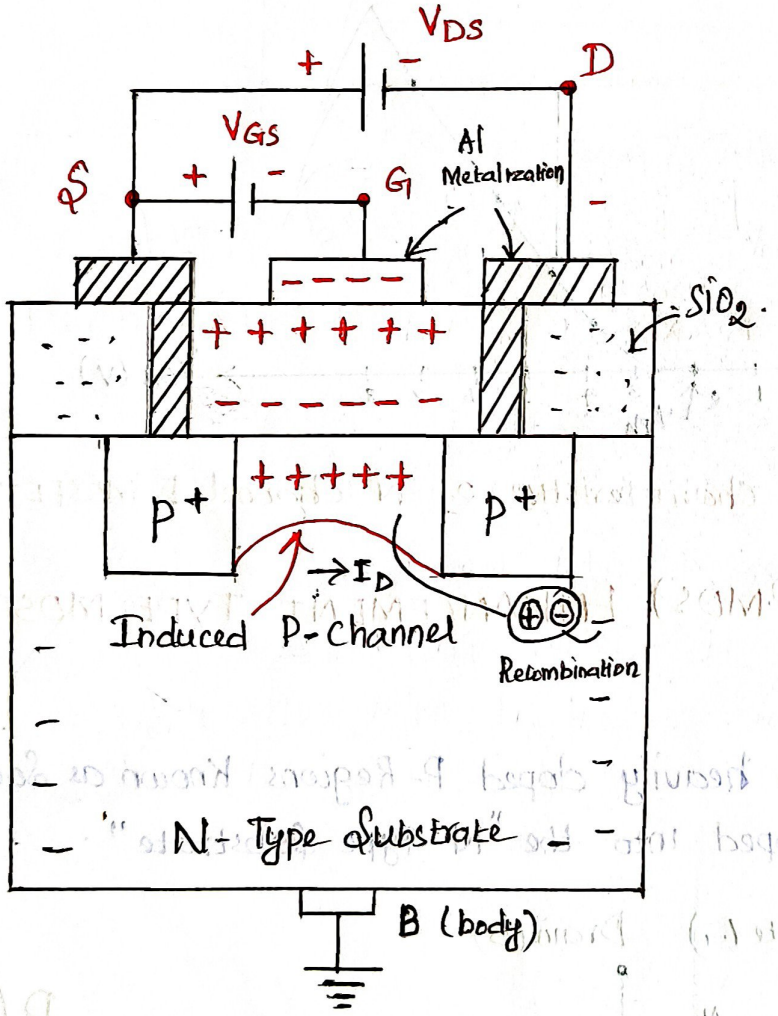


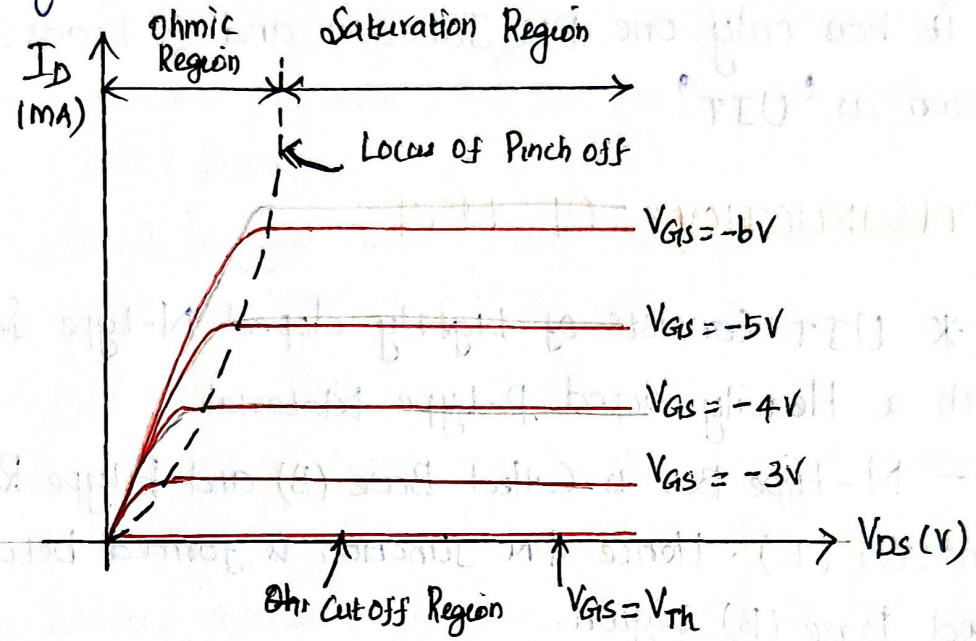
Fig. 2. P-channel E-MOSFET.

CHARACTERISTICS OF P-CHANNEL E-MOSFET

a) P-CHANNEL E-MOSFET DRAIN CHARACTERISTICS

In this case, V_{DS} and V_{GS} will be Negative and current will flow from Source to Drain terminal.

As V_{GS} becomes more and More Negative, drain Current (I_D) will increase and whenever $V_{GS} \lesssim V_{Th}$ MOSFET will operate in 'Cut-off Region'

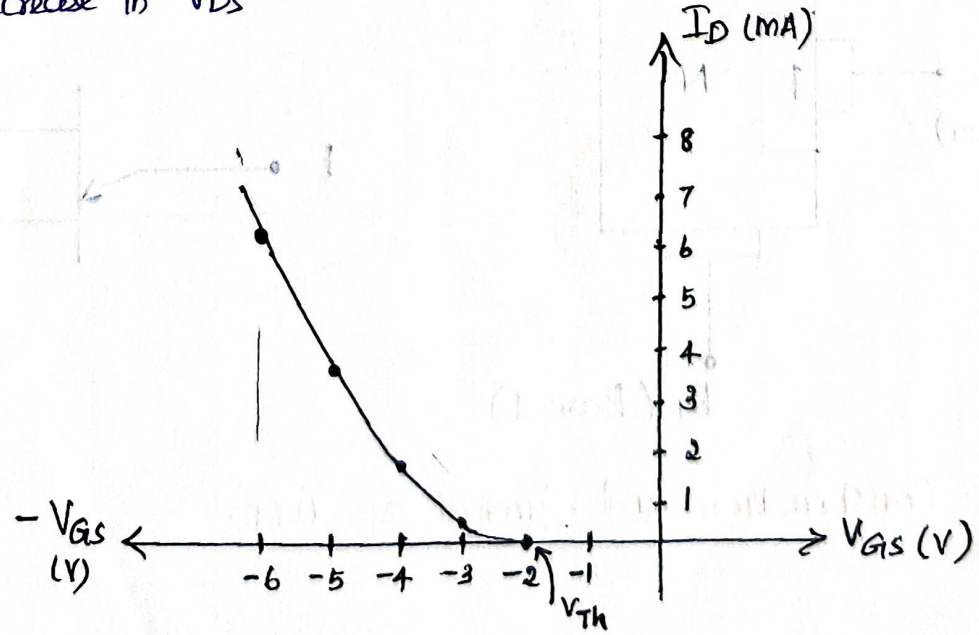


Fig·3· Drain characteristics of P-channel MOSFET.

b) P-CHANNEL E-MOSFET TRANSFER CHARACTERISTICS

The transfer characteristics of P-channel MOSFET is the Mirror image of 'N-channel E-MOSFET'.

* The drain current (I_D) is zero ($I_D = 0$) and the device remains OFF until V_{GS} reaches the $-V_{Th}$
- After this value I_D increases in the Reverse direction with a decrease in V_{DS}.



Fig·4· Transfer Characteristics of P-channel E-MOSFET.

UJT - UNI JUNCTION TRANSISTOR

UJT is a 3 terminal Semiconductor Switching device. As it has only one PN Junction and 3 Leads, it is commonly known as 'UJT'

1. CONSTRUCTION OF UJT

* UJT consists of Lightly doped N-type Semiconductor bar with a Heavily doped P-type Material.

- N-type Bar is Called Base (B) and P-type Region is Called Emitter (E). Hence PN Junction is formed between Emitter (E) and Base (B) region.

• Since Base (B) is lightly doped the Resistivity of the base material is very high. The direction of arrow head in the UJT Symbol represents the Conventional direction of Current flow when UJT is in Conduction State.

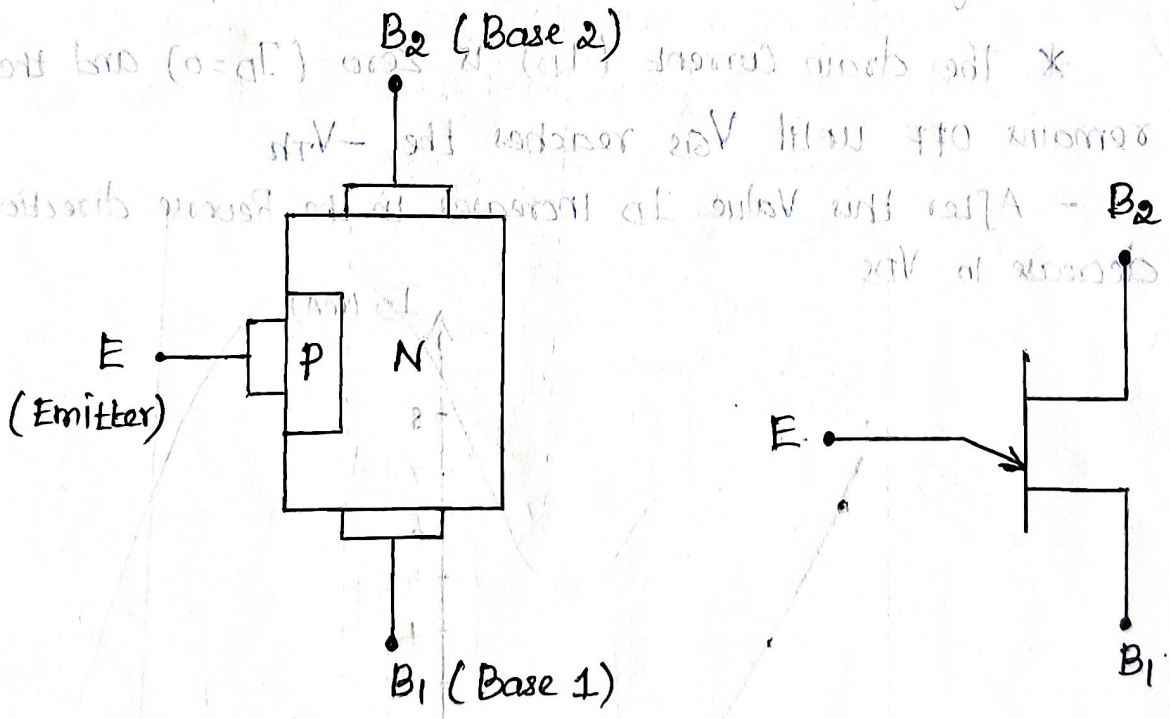


Fig.1. Construction and Symbol of UJT.

2. OPERATION / WORKING OF UJT

i) When No Voltage is applied at the Emitter (E) ('S' is open)

* When Switch is OPEN, Voltage V_{BB} is applied between the two Bases
* The Voltage drop, Reverse Bias the PN Junction and hence No Current ($I = 0$) flows.
* But a small leakage current flows from B_2 to Emitter (E) due to Minority Carriers. So UJT is in 'OFF State'.

ii) When a Positive Voltage is applied to the Emitter (E)

- When Switch (S) is closed, the PN Junction will remain Reversebiased as long as the Emitter Voltage (V_E) is less than V_1 ($V_E < V_1$)
- If the Emitter Voltage (V_E) is increased greater than V_1 ($V_E > V_1$) then PN Junction will be forward biased and holes are injected from P into N-type Silicon Base
- These holes are repelled by the Positive terminal 'B_2' and are attracted by the terminal 'B_1', So the Emitter Current I_E increases
- This Process will continue until a condition of 'Saturation' is reached. The device is now said to be in the 'ON State'.

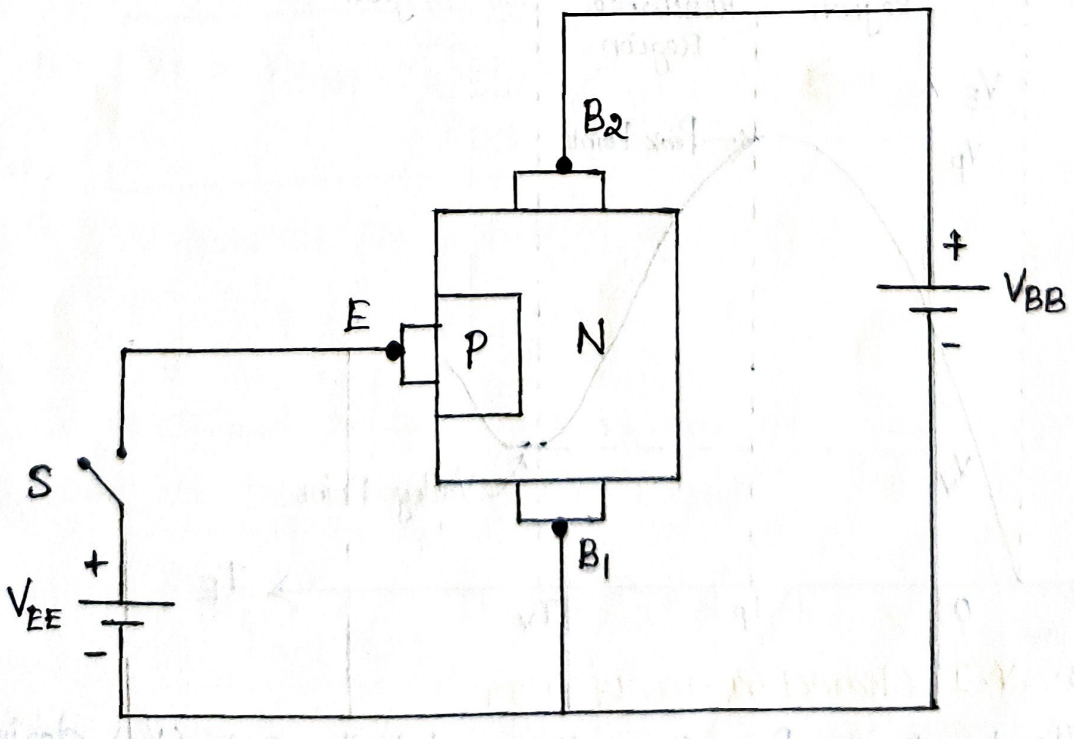


Fig. 2

iii) When a Negative Voltage is applied at the Emitter (E)

* If a Negative Voltage is applied to the Emitter (E), the PN Junction remains Reverse biased, the Emitter Current (I_E) is Cut-OFF.
* The device is now in the 'OFF State'.

3. CHARACTERISTICS OF UJT :

i) CUT-OFF REGION :

In this region V_E is below the Peak point and I_E is approximately Zero. ($I_E = 0$). UJT is in 'OFF State' in this region.

ii) NEGATIVE RESISTANCE REGION :

This is the region between Peak point (V_P) and Valley Point (V_V). In this region V_E decreases as I_E increases

* UJT is operated as an 'oscillator' in this region.

iii) SATURATION REGION :

This is the region beyond Valley Point (V_V). V_E almost remain Constant. In this region UJT is in 'ON State'.

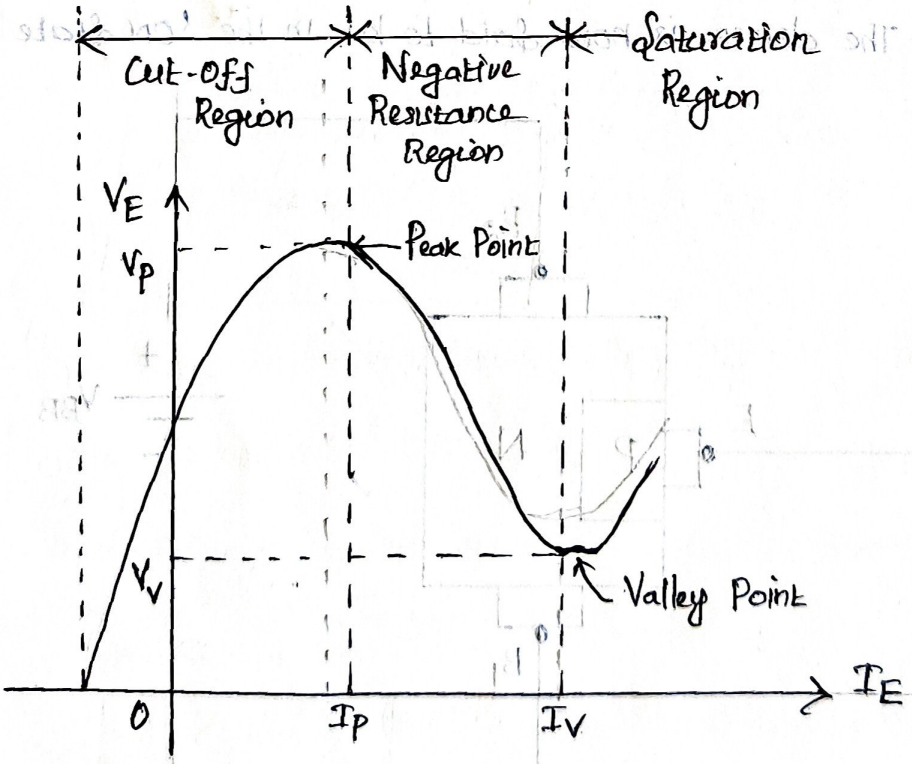


Fig. 3. V-I Characteristics of UJT.

The two points, Peak Point (V_P) and Valley Point (V_V) derive three important Region in V-I characteristics as shown in fig. 3.

4. EQUIVALENT CIRCUIT OF UJT / BIASING OF THE UJT.

Equivalent Circuit of UJT consists of a PN diode (D) with a Resistance (R_{BB}) represents Internal Bulk Resistance or Inter Base Resistance.

- It is the Total Resistance between Base terminals (B_1, B_2)

The sum of R_{B1} and R_{B2} is called 'R_{BB}'

* The P-type Emitter forms a PN Junction with the N-type silicon Bar and this junction is shown as a diode (D_1) in the equivalent circuit.

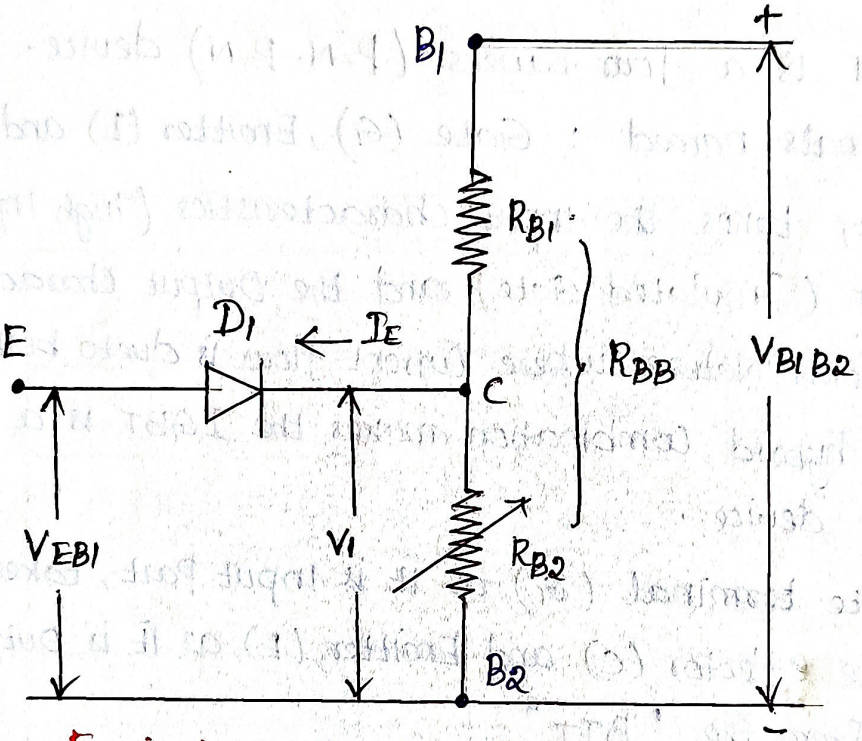


Fig.4. Equivalent Circuit of UJT.

$$V_1 = V_{B1B2} \times \frac{R_{B1}}{R_{BB}}$$

Where,

V_1 - Voltage at the Cathode of the diode.

INTRINSIC STANDOFF RATIO (η) :

It is defined as the Ratio between the Internal dynamic Resistance (R_{B1}) and the Inter Base Resistance (R_{BB})

$$\eta = \frac{R_{B1}}{R_{B1}+R_{B2}} \qquad (R_{BB} = R_{B1}+R_{B2})$$

V_{RB} - Intrinsic stand off Voltage.

Intrinsic Stand off Ratio denoted by η and it is important in UJT characteristics The Value of Intrinsic stand off Ratio lies between 0.5 to 0.8

IGBT - INSULATED GATE BIPOLAR TRANSISTOR

IGBT is a Semiconductor Switching device. MOSFET and BJT are the most used electronic Semiconductor device.

* IGBT is designed with the characteristics of Both MOSFET and BJT. IGBT is a combination of MOSFET and BJT.

1. CONSTRUCTION OF IGBT

IGBT is a four Layers (P-N-P-N) device. IGBT has three terminals named : Gate (G), Emitter (E) and Collector (C).

* IGBT takes the input characteristics (High input Impedance) of MOSFET (Insulated Gate) and the Output Characteristics of BJT (Bipolar Nature where Current flow is due to both charge carriers)

- This hybrid combination makes the IGBT is a Voltage - Controlled device.

* Gate terminal (G) as it is input part, taken from 'MOSFET' while the Collector (C) and Emitter (E) as it is output part, taken from the 'BJT'.

i) The Collector (C) electrode is attached to P-Layer or 'P-Substrate'. While the Emitter (E) is attached between the P and N-Layers.

ii) A P+ Substrate is used for the construction of IGBT. An N- Layer is placed on top of it to form PN Junction 'J1' i.e., The Junction between the P-Layer and N- Layer is called Junction 2 (J2)

iii) the Junction between the P-Substrate and N⁻ Layer is Called Junction 1 (J1).

iv) Emitter (E) is directly attached to the N+ Region while the Gate (G) is insulated using SiO_2

The Base P+ Substrate inject holes into N^- Layer that is why it is Called 'Injection Layer' while the N^- Layer is called 'drift Region'. The P-Layer above is known as the 'Body Region'

* The 'N+ Buffer Layer' between the P+ Substrate and N^- Layer is not essential for the operation of IGBT.

- IGBTs with Buffer Layer are termed as 'Punch-Trough (PT) IGBT
- IGBTs without Buffer Layer are termed as 'Non-Punch-Trough (NPT) IGBT

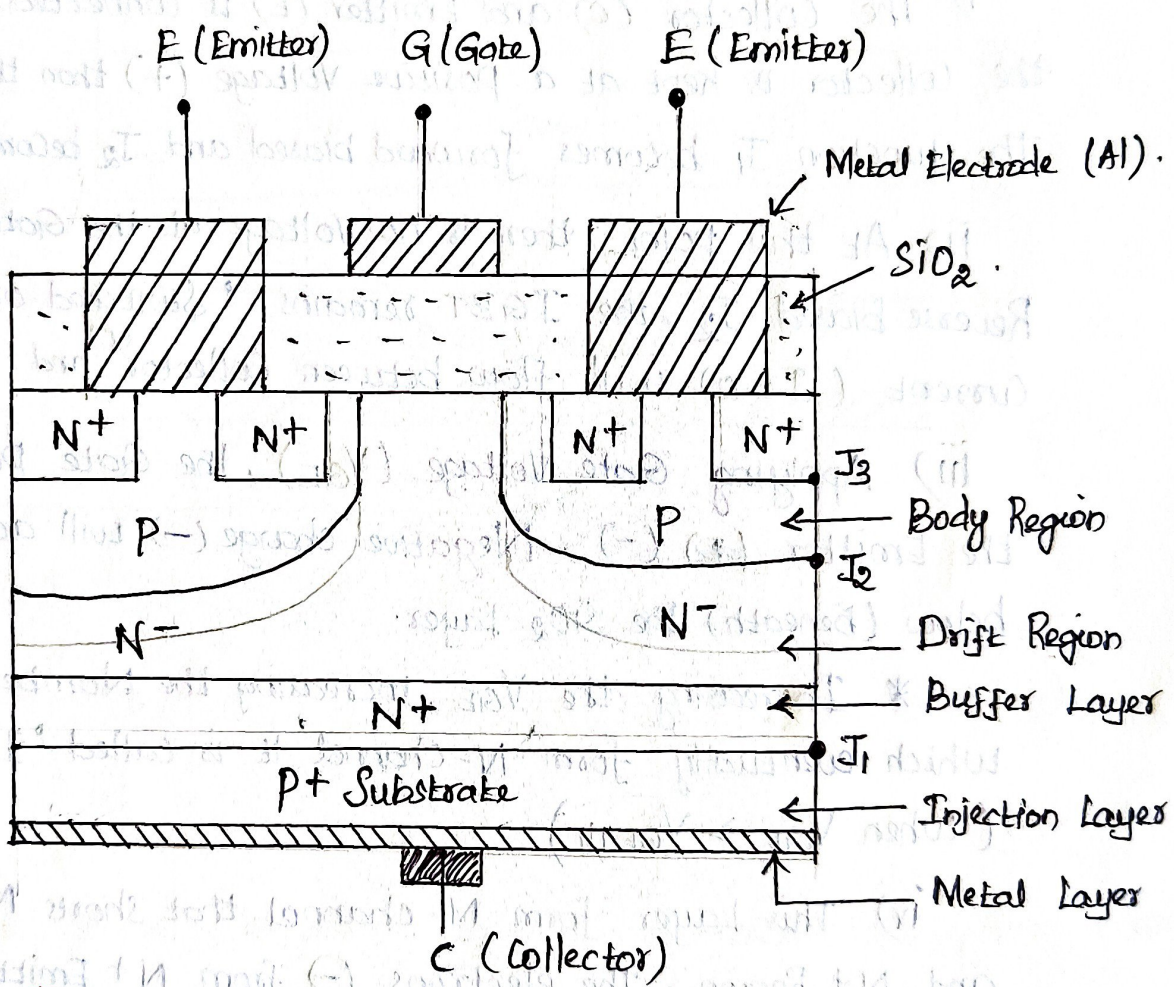


Fig. 1. IGBT Constructional Structure.

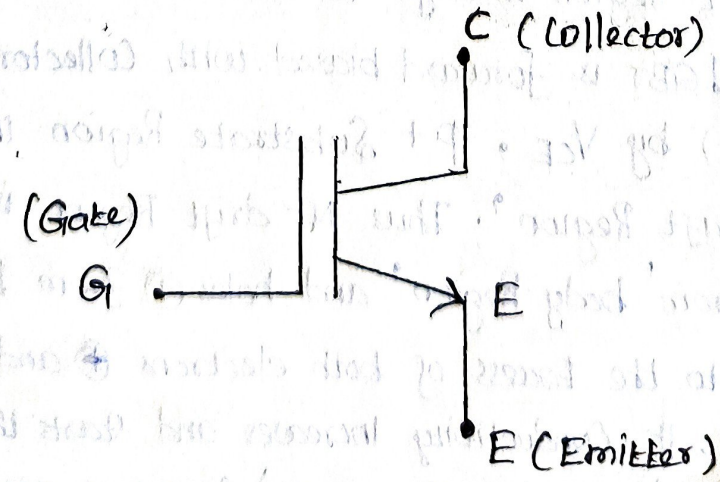


Fig. 2. Symbol of IGBT.

2. WORKING PRINCIPLE OF IGBT

* The two terminals of IGBT Collector (C) and Emitter (E) are used for the conduction of current (I) while the Gate (G) is used for controlling the 'IGBT'

- Its working is based on the biasing between Gate-Emitter terminals (V_{GE}) and Collector-Emitter terminals (V_{CE}).

i) The Collector (C) and Emitter (E) is connected to 'V_{CE}' such that the Collector is kept at a positive voltage (+) than the Emitter (-). The junction J_1 becomes forward biased and J_2 become Reverse biased.

ii) At this point, there is no voltage at the Gate (G). Due to Reverse biased J_2, the IGBT remains 'Switched-OFF' and No current ($I=0$) will flow between Collector (C) and Emitter (E).

iii) Applying Gate voltage (V_{GE}), the Gate positive (+) than the Emitter (E) (-), Negative charge (-) will accumulate just below (beneath) the SiO_2 layer.

* Increasing the V_{GE}, increasing the Number of charges which eventually form 'N-channel' IE is called 'Inversion Layer' (when $V_{GE} > V_{GE\,Th}$)

iv) This Layer form N-channel that shorts N- drift Region and N+ Region. The electrons ⊖ from N+ Emitter begins to flow to N⁻ drift Region through 'N-channel'

v) As IGBT is forward biased with Collector (+) (positive) and Emitter Negative (-) by V_{CE}, P+ Substrate Region injects holes ⊕ into 'N⁻ drift Region'. Thus N⁻ drift Region is flooded with (e^- or -) electrons from 'body Region' and holes ⊕ from P+ Substrate Region.

vi) Due to the Excess of both electrons ⊖ and holes ⊕ in the drift Region, its Conductivity increases and starts the Conduction of Current (I). Hence the IGBT is 'Switched-ON'

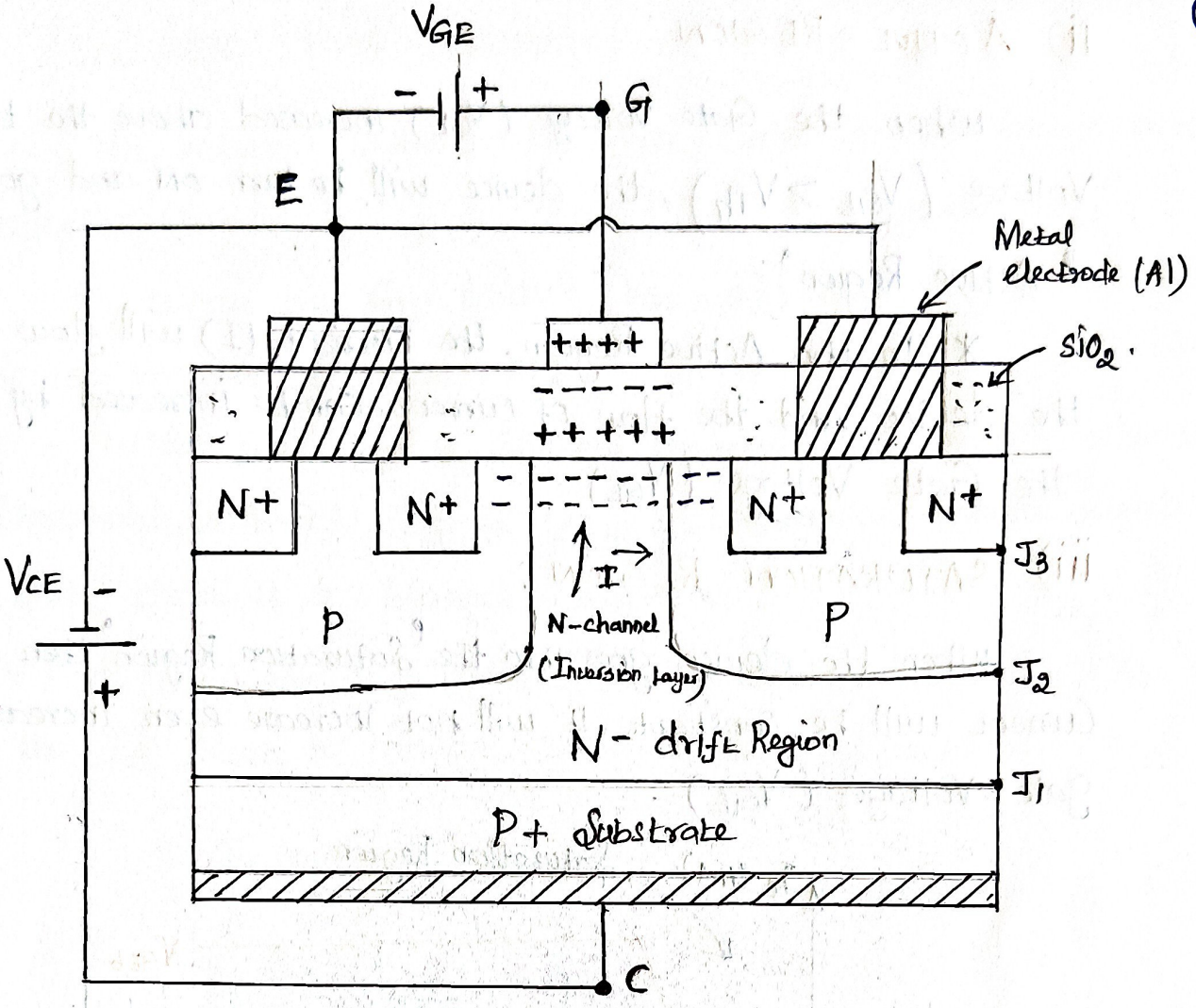


Fig. 3. Working of IGBT.

3. CHARACTERISTICS OF IGBT

a) STATIC CHARACTERISTICS OF IGBT (OUTPUT CHARACTERISTICS).

The Y-axis represents the Collector Current (I_C) and X-axis represents the Collector-Emitter Voltage (V_{CE}). We can see the Output characteristics of the IGBT.

i) CUT-OFF REGION:

When the Gate Voltage (V_{GE}) is Zero ($V_{GE} = 0$), then the device is in the 'OFF State' this is called 'Cut-off Region'.

*) When the Gate Voltage increased but below threshold Voltage ($V_{GE} < V_{Th}$), there will be a Small Leakage Current but then also the device will be in the 'Cut-off Region'.

ii) ACTIVE REGION :

When the Gate Voltage (V_{GE}) increased above the threshold Voltage ($V_{GE} > V_{Th}$), the device will be turn-ON and goes into 'Active Region'.

* In this Active Region, the Current (I) will flow through the device and the flow of current can be increased by increasing the Gate Voltage (V_{GE}).

iii) SATURATION REGION :

When the device goes into the 'Saturation Region' then the flow of Current will be constant. It will not increase even increasing the gate Voltage (V_{GE}).

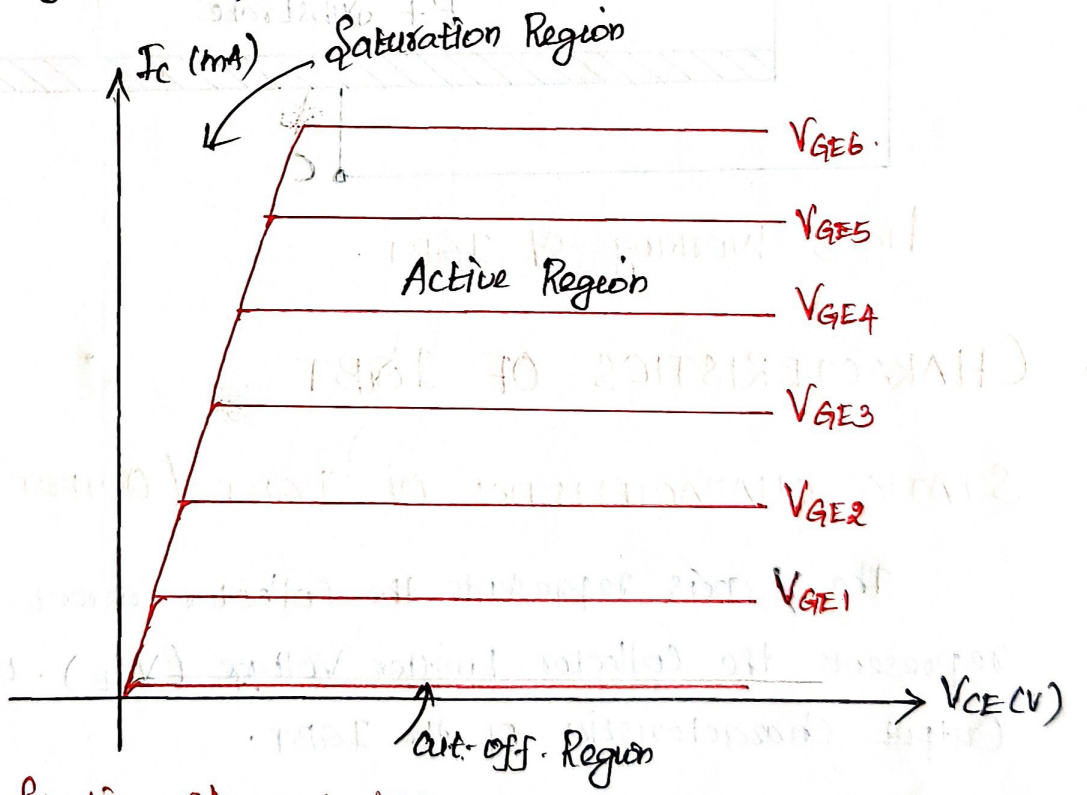


Fig. 4. Static Characteristics of IGBT.

The shape of the Output characteristics is similar to the 'BJT'. But here the controlling Parameter is 'V_{GE}' because IGBT is a "Voltage-Controlled device"

The Transfer characteristics of IGBT is similar to the MOSFET

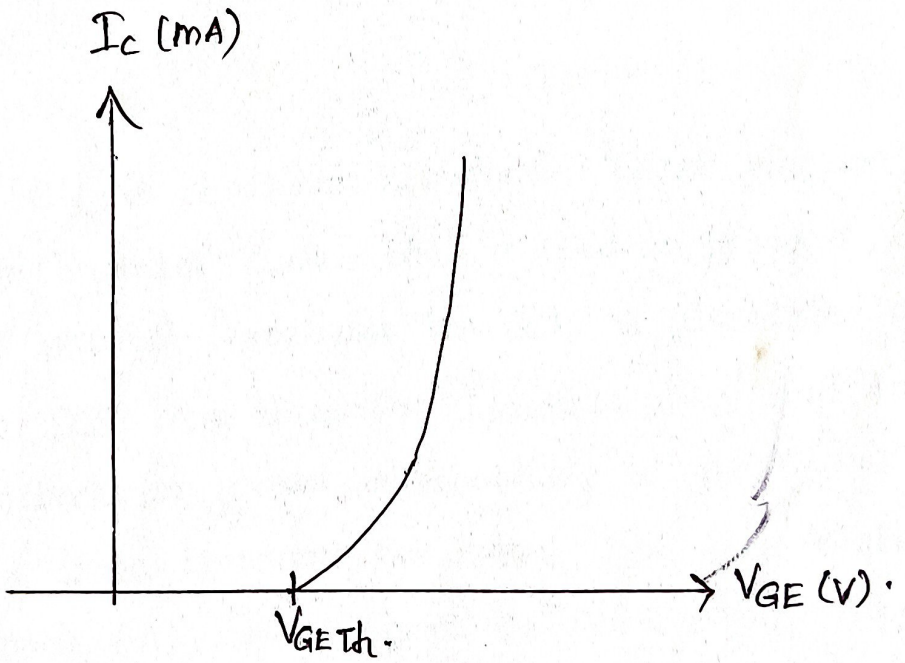
b) TRANSFER CHARACTERISTICS OF IGBT

The relation between the (V_{GE}) Gate-Emitter voltage and Collector Current (I_C) is called 'Transfer characteristics' of IGBT.

* When the V_{GE} is 0V ($V_{GE} = 0$), there is no I_C and the device remains switched-OFF.

- When the V_{GE} is slightly increased but remains below the threshold voltage ($V_{GE} < V_{GE\,Th}$), the device remains 'switch-OFF' but there is a Leakage Current.

* When the V_{GE} exceeds the threshold limit ($V_{GE} > V_{GE\,Th}$), the I_C starts to increase and the device 'switch-ON'



SCR - SILICON CONTROLLED RECTIFIER [THYRISTOR]

INTRODUCTION :

The Silicon Controlled Rectifier (SCR) is the most important and mostly used member of the thyristor Family.

- SCR can be used for different applications like Rectification, Regulation of power and Inversion, etc.,.

* Like a diode, SCR is a Unidirectional device that allows the Current in one direction and opposes in another direction.

• SCR is a three terminal device ; Anode, Cathode and Gate. SCR has built in feature to turn ON or OFF and its Switching is Controlled by biasing conditions and Gate Input terminal

CONSTRUCTION OF SCR : (THYRISTOR)

An SCR is a three terminal, Three junction, and four Layer Semiconductor device that is used to perform Switching functions in power circuits. Sometimes the SCR is also called as 'Thyristor'.

- The SCR has three PN Junctions, and Four Layer of P and N type Semiconductor joined alternatively to get PNPN device.

* The three terminals are taken, one from Outer P-type Layer Called Anode (A), Second from the Outer N-type layer called Cathode (K) and the third from the Internal P-type layer called Gate (G).

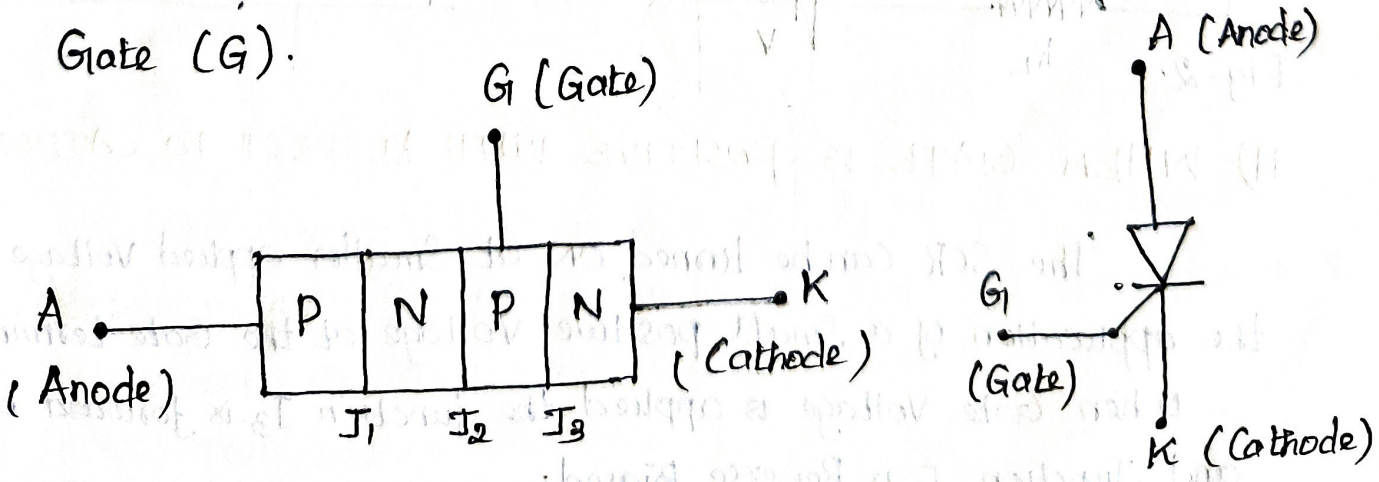


Figure.1. Construction and Symbol of SCR

WORKING OF SCR :

In a SCR, the Load is Connected in Series with the Anode. The anode is always kept positive with respect to Cathode

i) WHEN GATE IS OPEN CIRCUITED :

When No Voltage applied to Gate terminal, Junction J_2 is Reverse biased and the junctions J1 and J3 are Forward biased.

- Since one of the three junctions is Reverse biased so there is No Current ($i=0$) can flow through the Load, hence the SCR is OFF However if the applied Voltage is gradually increased, the stage is reached, when Reverse biased junction (J_2) breaks down.

* The SCR now, Starts Conducting and become ON. The Value of applied Voltage at which the Reverse Biased junction breaks down and the SCR becomes ON is known as 'Break over Voltage'.

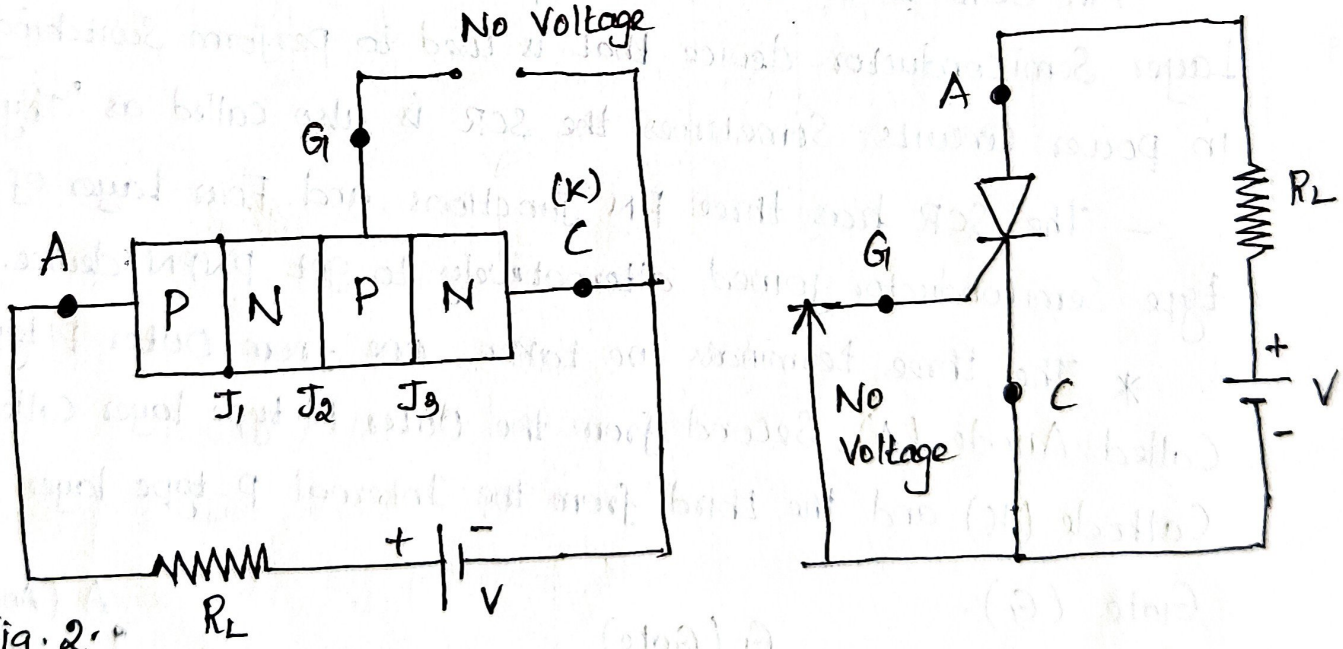


Fig. 2.

ii) WHEN GATE IS POSITIVE WITH RESPECT TO CATHODE

The SCR can be turned ON at Smaller applied Voltage by the application of a Small positive Voltage at the Gate terminal.

- When Gate Voltage is applied the junction J_3 is forward biased and Junction J_2 is Reverse Biased.

Thus, the electrons from N-type layer starts moving across the Junction J_3 toward p-type material and the holes from P-type material towards the N-type material.

* Due to the movement of holes and electrons across the junction J_3, the Gate Current (i_G) starts flowing. Because of gate current the Anode Current (i_A) increases

- The increased Anode Current makes the more electrons available at the junction J_2. As a result of this process, in a small time, the Junction J_2 breaks down and the SCR is turn ON.

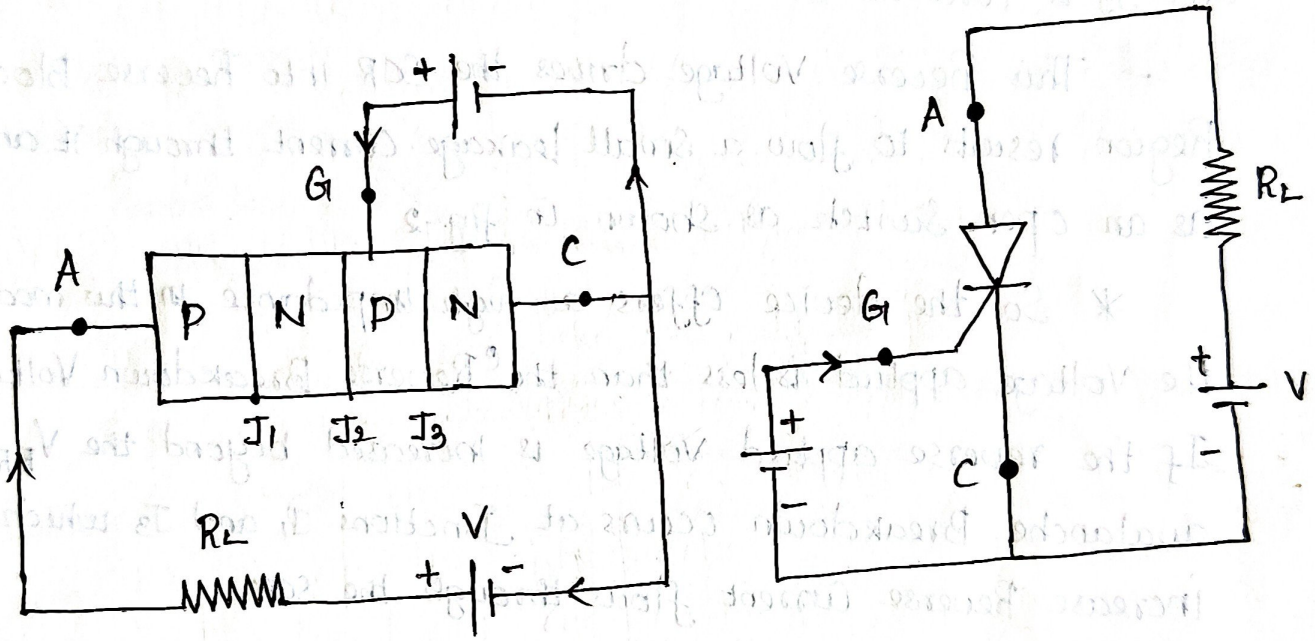


Fig. 3.

- Even if the Voltage at the Gate terminal (G) is Removed, the SCR the Anode Current (i_A) does not decrease. The SCR can only be turned OFF by reducing the Applied Voltage to zero.

STATIC ANODE-CATHODE (V-I) CHARACTERISTICS OF SCR

The Static V-I characteristics of an SCR is shown in fig.4. Depending on the Biasing given to the SCR, the operation of SCR is divided into three modes.

- They are :

MODES OF OPERATION OF SCR

1. Reverse Blocking Mode
2. Forward Blocking Mode
3. Forward Conduction Mode.

1. REVERSE BLOCKING MODE :

In this mode of operation, Cathode (K) is made positive with respect to Anode (A). Then the junctions J_1 and J_3 are Reverse biased and J_2 is Forward Biased.

– This Reverse Voltage drives the SCR into Reverse Blocking Region results to flow a small leakage current through it and acts as an open switch as shown in fig-2

* So the device offers a high impedance in this mode until the voltage applied is less than the 'Reverse Breakdown Voltage' V_{BR} If the reverse applied voltage is increased beyond the V_{BR}, then avalanche Breakdown occurs at Junctions J_1 and J_3 which results to increase Reverse current flow through the SCR.

– This Reverse Current cause more losses in the SCR and even to increase the heat of it. So there will be a considerable damage to the SCR when the Reverse Voltage applied more than V_{BR}

2. FORWARD BLOCKING MODE :

In this mode of operation, the Silicon Controlled Rectifier is Connected such that the Anode (A) Terminal is made positive with respect to cathode (K) while the Gate Terminal (G) kept open.

– In this state junctions J_1 and J_3 are Forward biased and the junction J_2 is Reverse Biased. Due to this, a small Leakage Current flows through the SCR, until the voltage applied across

the SCR is more than the Breakover Voltage of it, SCR offers a Very high Resistance to the Current flow.

— Therefore, the SCR acts as a open Switch in this mode by Blocking forward current flowing through the SCR as shown in the VI characteristics Curve of the SCR

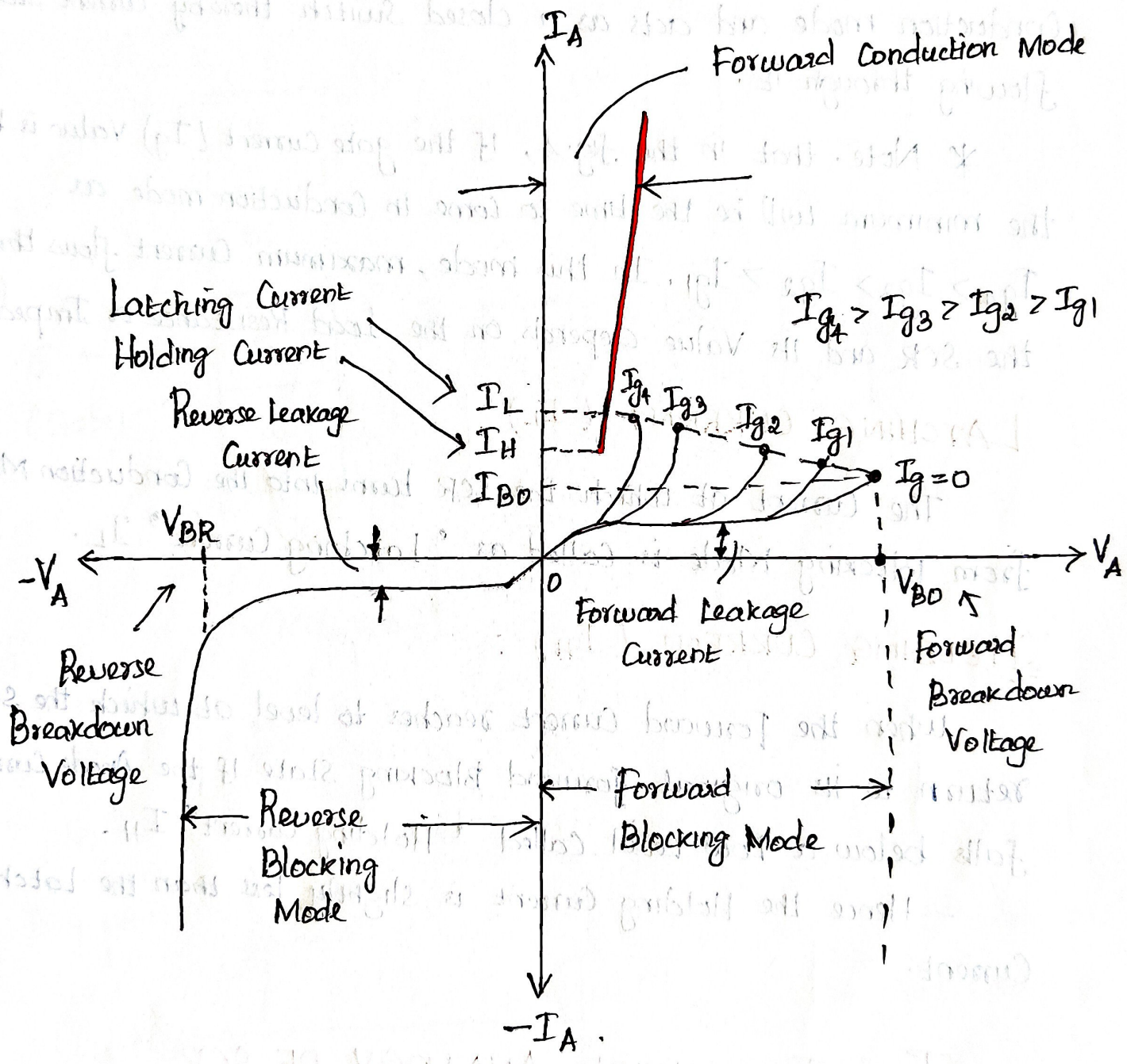


Fig. 4. V-I characteristics of SCR

3. FORWARD CONDUCTION MODE :

In this mode, SCR or Thyristor Comes into the Conduction mode from Blocking mode.

It can be done in two ways as either by applying positive pulse to gate terminal or by increasing the forward voltage beyond the Breakover voltage of the SCR (V_{BR}).

- Once any one of these methods is applied, the avalanche Breakdown occurs at junction J_2. Therefore the SCR turns into the Conduction mode and acts as a closed switch thereby current starts flowing through it.

* Note. that in the fig. 4, If the gate current (I_g) value is high, the minimum will be the time to come in Conduction mode as $I_{g4} > I_{g3} > I_{g2} > I_{g1}$. In this mode, maximum current flows through the SCR and its value depends on the load Resistance or Impedance.

LATCHING CURRENT (I_L):

The current at which the SCR turns into the Conduction Mode from Blocking Mode is called as 'Latching Current' I_L.

HOLDING CURRENT (I_H):

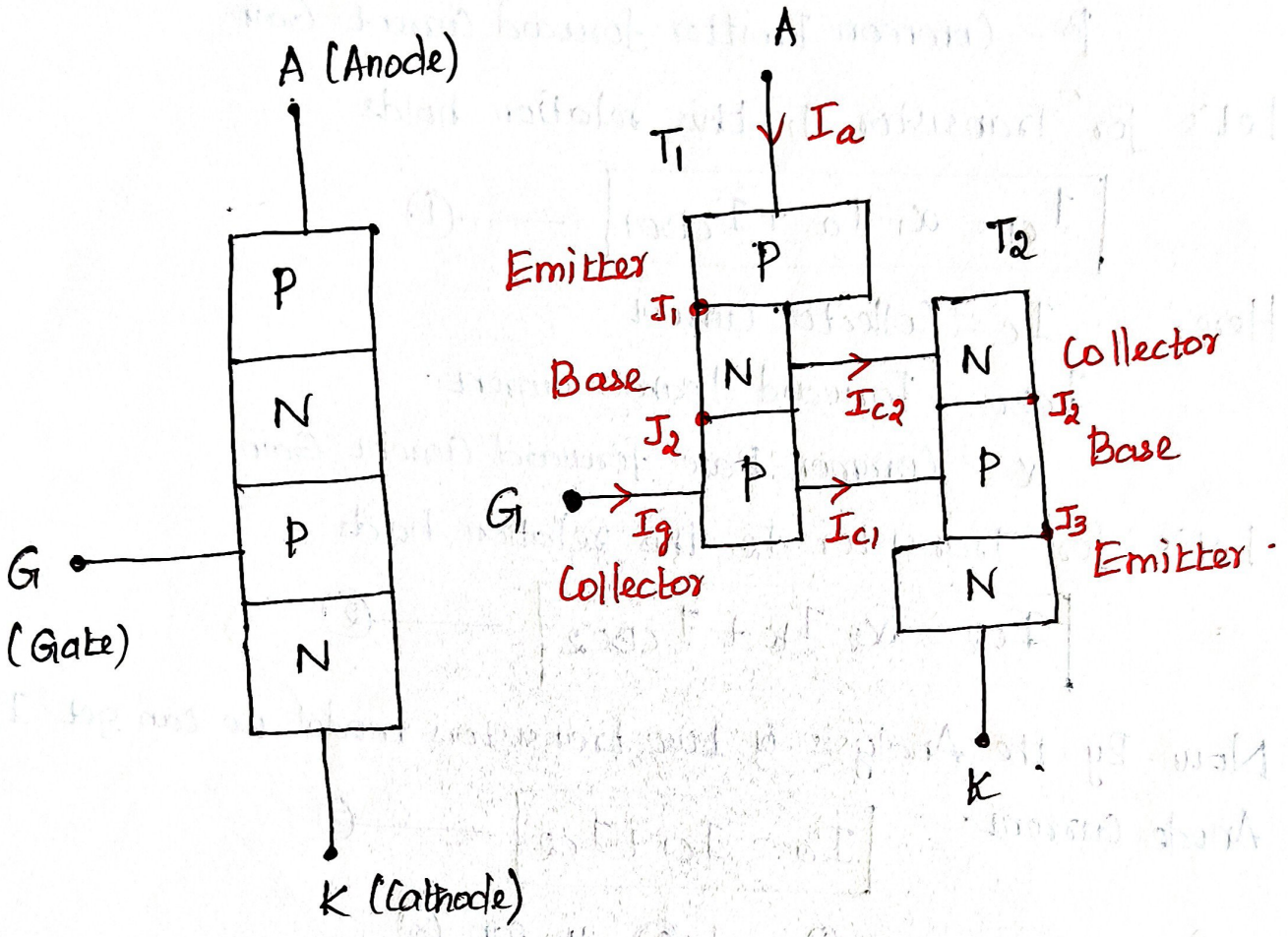
When the forward current reaches to level at which the SCR return to its original forward Blocking state If the Anode current falls below a low level called 'Holding Current' I_H.

- Hence the Holding current is slightly less than the Latching current.

TWO TRANSISTOR ANALOGY OF SCR

Two transistor Analogy of SCR is a method of representing SCR in the form of two Transistor model. This represents SCR is the combination of PNP and NPN Transistor.

SCR or Thyristor is the three terminal Semiconductor device which having P-N-P-N Structure. The Basic operating principle of SCR can understand by Two transistor Method of SCR.



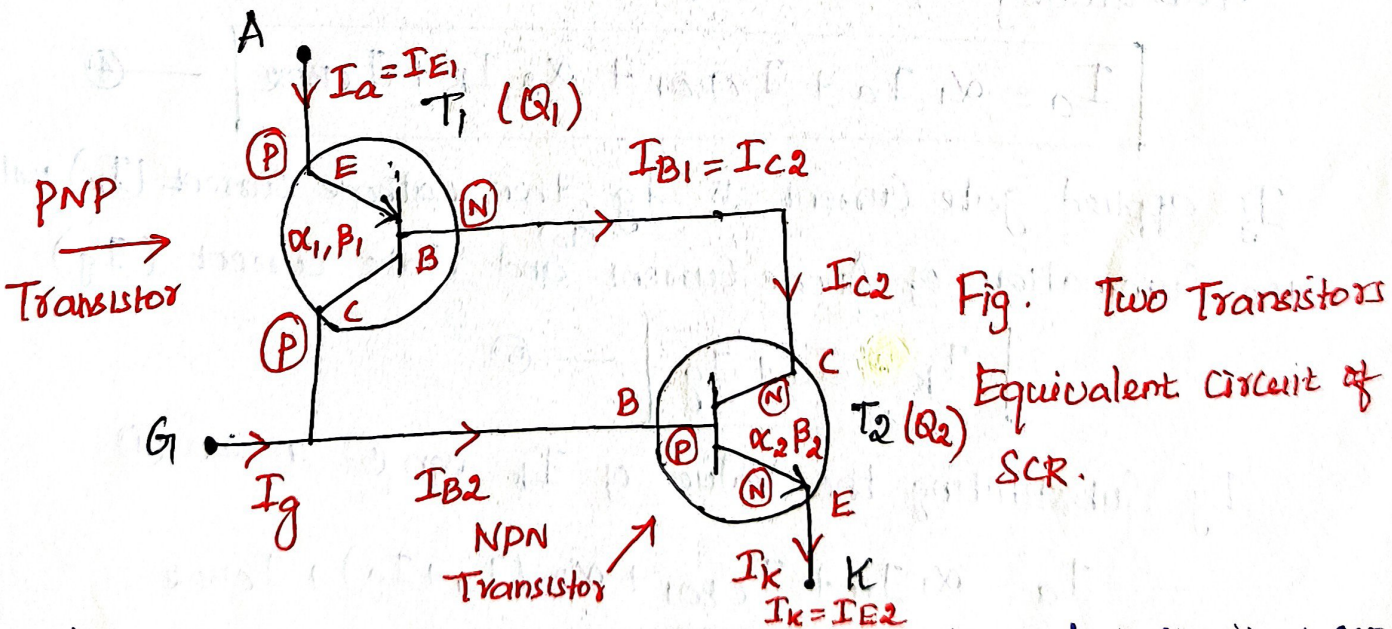


Fig. Two Transistors Equivalent Circuit of SCR.

As per figure you can see Two Transistors Equivalent Circuit of SCR. From the figure, Base of the Transistor T_1 is work as the collector of the Transistor T_2. and collector of the Transistor T_1 work as the Base of the Transistor T_2.

The relation between I_C and I_B is

$$\boxed{I_C = \beta I_B}$$

where, I_B - Base Current

β - Common Emitter forward Current Gain

Let's for Transistor T_1 this relation holds

$$\boxed{I_{C1} = \alpha_1 I_a + I_{CBO1}} \quad \text{——} (1)$$

Here, I_C - Collector Current

I_{CBO} - Forward Leakage Current.

α - Common Base forward Current Gain

Let's for Transistor T_2 this relation holds

$$\boxed{I_{C2} = \alpha_2 I_k + I_{CBO2}} \quad \text{——} (2)$$

Now, By the Analysis of two transistors model we can get I_a Anode current.

$$\boxed{I_a = I_{C1} + I_{C2}} \quad \text{——} (3)$$

Substituting eqn (1) and (2) in eqn (3)

$$\boxed{I_a = \alpha_1 I_a + I_{CBO1} + \alpha_2 I_k + I_{CBO2}} \quad \text{——} (4)$$

If applied gate Current is I_g, then Cathode Current (I_k) will be the Summation of Anode Current (I_a) and Gate Current (I_g)

$$\boxed{I_k = I_a + I_g} \quad \text{——} (5)$$

By Substituting the Value of I_k eqn (5) in eqn (4)

$$I_a = \alpha_1 I_a + I_{CBO1} + \alpha_2 (I_a + I_g) + I_{CBO2}$$

finally $$\boxed{I_a = \frac{\alpha_2 I_g + I_{CBO1} + I_{CBO2}}{1 - (\alpha_1 + \alpha_2)}}$$

From this relation we can assure that with increasing the Value of $(\alpha_1 + \alpha_2)$ towards unity, Corresponding Anode Current will increase.

UNIT - III AMPLIFIERS

A. JEYARAJ AP/EEE

INTRODUCTION

An Amplifier is defined as the device which increase the magnitude of the input signal and produces a larger electrical output

* The Amplifier needs a source of energy for amplification from Battery or dc source and Filter combination. The amplifier also has atleast one active devices such as BJT, FET or Electron tube.

TYPES OF AMPLIFIERS

If the output signal is directly proportional to the corresponding Input signal, then the amplifier is called 'LINEAR AMPLIFIER'

- If the output signal is not directly proportional to the corresponding Input signal, then the amplifier is called 'Non-Linear Amplifier'.

Now let us discuss the operation of small signal Amplifiers and analyze its performance.

SMALL SIGNAL AMPLIFIERS

Small signal indicates that the input signal is very small in the range of few mV. The amplifier which operates on small signal is called 'Small signal Amplifier'.

- As the input signal is small, the transistor will operate in the Linear Region of its transfer characteristics. So it is called 'Linear Amplifier'. The output signal will not have any distortion

EXAMPLE :

CE, CB and CC Amplifier.

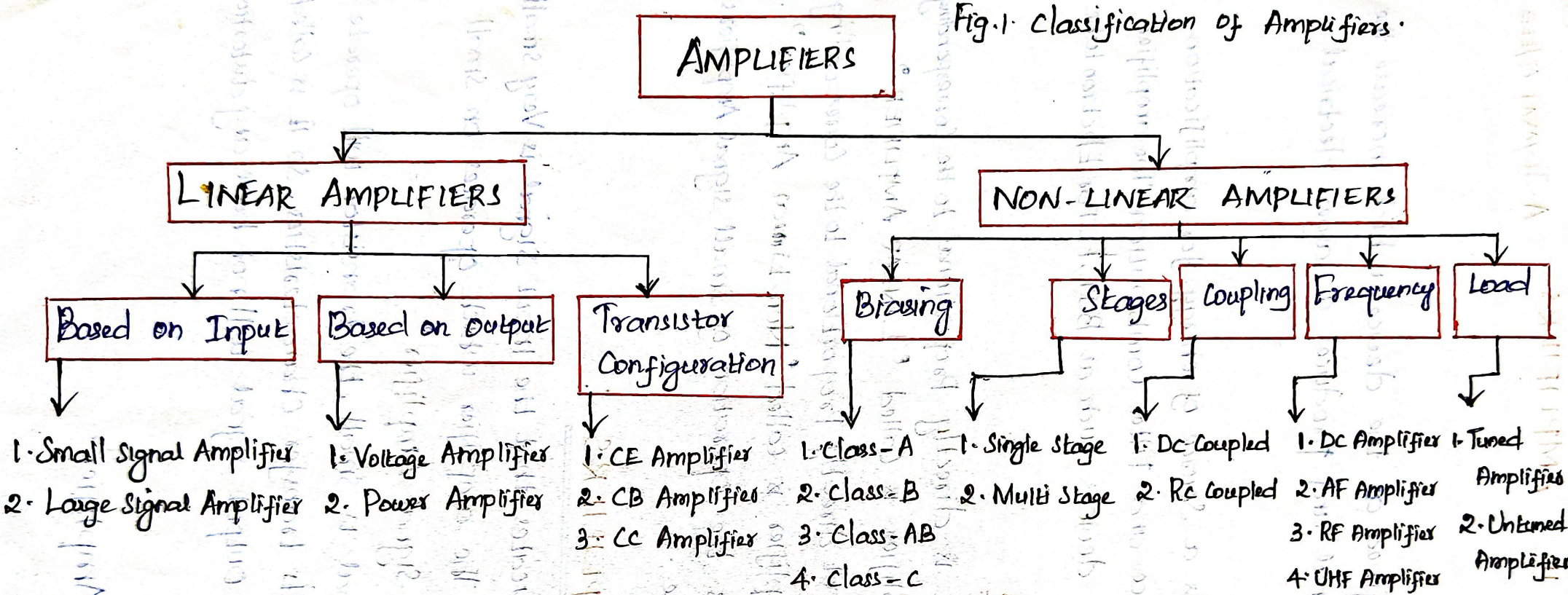


Fig.1. Classification of Amplifiers.

TRANSISTOR AS A TWO PORT DEVICE

A transistor can be treated as a two-port Network. The Voltage and current at port 1 are V_1 and i_1 and the Voltage and current at port 2 are V_2 and i_2 as shown in fig. 1.

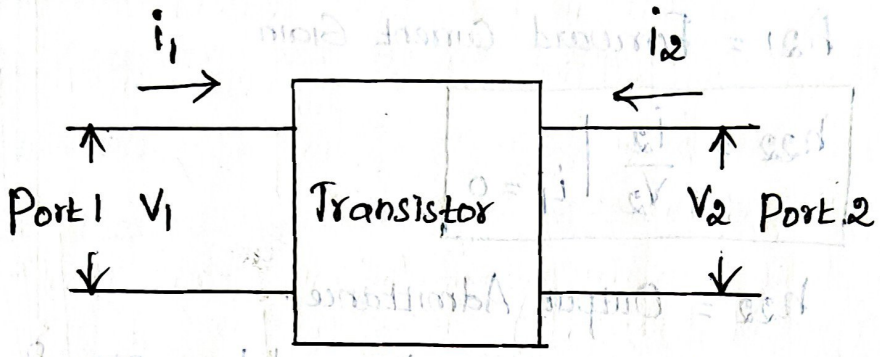


Fig. 1. Transistor as a two port device.

* Any two parameters are considered to be independent Variables and the other two parameters are expressed in terms of the Independent Variables.

HYBRID PARAMETERS

The hybrid or h parameters are used for analysis of the Transistor.

* If the input Current i_1 and the Output Voltage V_2 are taken as independent Variables, then the input Voltage V_1 and Output Current i_2 are expressed in terms of i_1 and V_2.

Since the units of the four parameters are Completely different from each other, these parameters are called 'Hybrid Parameters'.

$$V_1 = h_{11} i_1 + h_{12} V_2$$

$$i_2 = h_{21} i_1 + h_{22} V_2$$

The four hybrid parameters $h_{11}, h_{12}, h_{21}, h_{22}$ are defined as

$$h_{11} = \left.\frac{V_1}{i_1}\right|_{V_2 = 0}$$

h_{11} = Input Impedance with Output Port Short Circuited.

$$h_{12} = \left.\frac{V_1}{V_2}\right|_{i_1=0}$$

h_{12} = Reverse Voltage Transfer Ratio.

$$h_{21} = \left.\frac{i_2}{i_1}\right|_{V_2=0}$$

h_{21} = Forward Current Gain

$$h_{22} = \left.\frac{i_2}{V_2}\right|_{i_1=0}$$

h_{22} = Output Admittance.

The units of the h-Parameters h_{11} and h_{22} are Ω and mho respectively h_{12} and h_{21} are dimensionless.

* As the units of h-parameters are different they are called 'hybrid Parameters'. The Values of h-parameters depend upon

1. Transistor type
2. Transistor Configuration
3. Operating point
4. Frequency
5. Temperature

ADVANTAGES OF h-Parameters

1. Easy to measure from Static Characteristics of Transistor
2. Simple Conversion from one Configuration to Other.
3. Used upto Radio frequencies.
4. Convenient for Circuit Analysis and Design

SMALL SIGNAL ANALYSIS

The operation of an Amplifiers in the mid band Region of its frequency Response is analyzed. So it is called 'Mid band Analysis'

ASSUMPTIONS :

1. All the coupling and Bypass Capacitors are equivalent to 'Short circuit'
2. All the internal Capacitances of the Transistor are 'open-circuited'

STEPS :

1. Draw the ac equivalent circuit of the Amplifiers.
2. Draw the Hybrid Equivalent Circuit.
3. Calculate Input Impedance, Output Impedance, Current Gain, Voltage Gain and power Gain of the Amplifier.

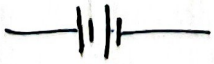
ANALYSIS OF CE AMPLIFIER

Let us analysis the Common Emitter (CE) Amplifier as follows.

STEP : 1

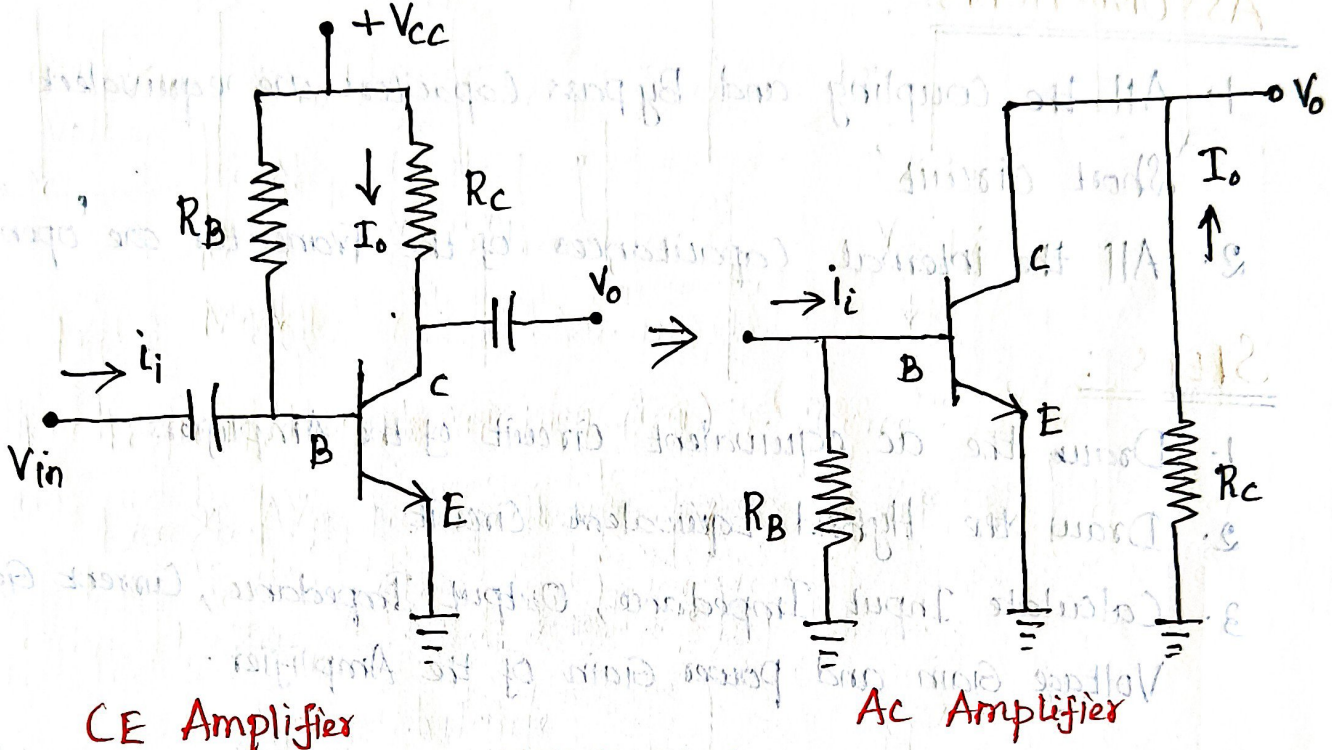
Draw ac equivalent Circuit of the Amplifier. Table-1 shows the ac equivalent circuit for different dc elements.

Table-1 Dc and Ac Equivalent Circuit for different Elements

Element	Dc Model	Ac Model
Resistor		
Capacitor		
Inductor		
Voltage Source		
Current Source		

To draw the ac equivalent circuit of the amplifier, the following steps should be followed.

1. Replace the dc voltage source by a short circuit.
2. Replace coupling and Bypass capacitor by the short circuit.



CE Amplifier Ac Amplifier

Fig. 1. CE Amplifier and its Ac equivalent circuit.

STEP : 2

Hybrid Equivalent Circuit

From the Ac equivalent circuit, the hybrid equivalent circuit can be obtained as shown in fig. 2. The below figure. 2 can also be drawn as in fig. 3 by connecting the common Ground.

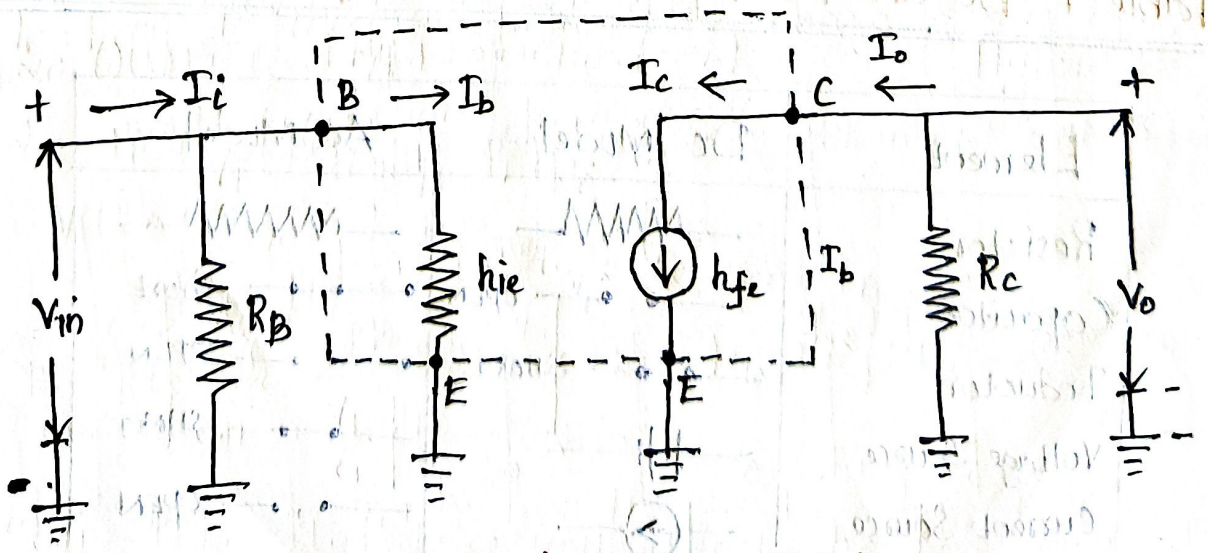


Fig. 2 Hybrid Ac Equivalent Circuit.

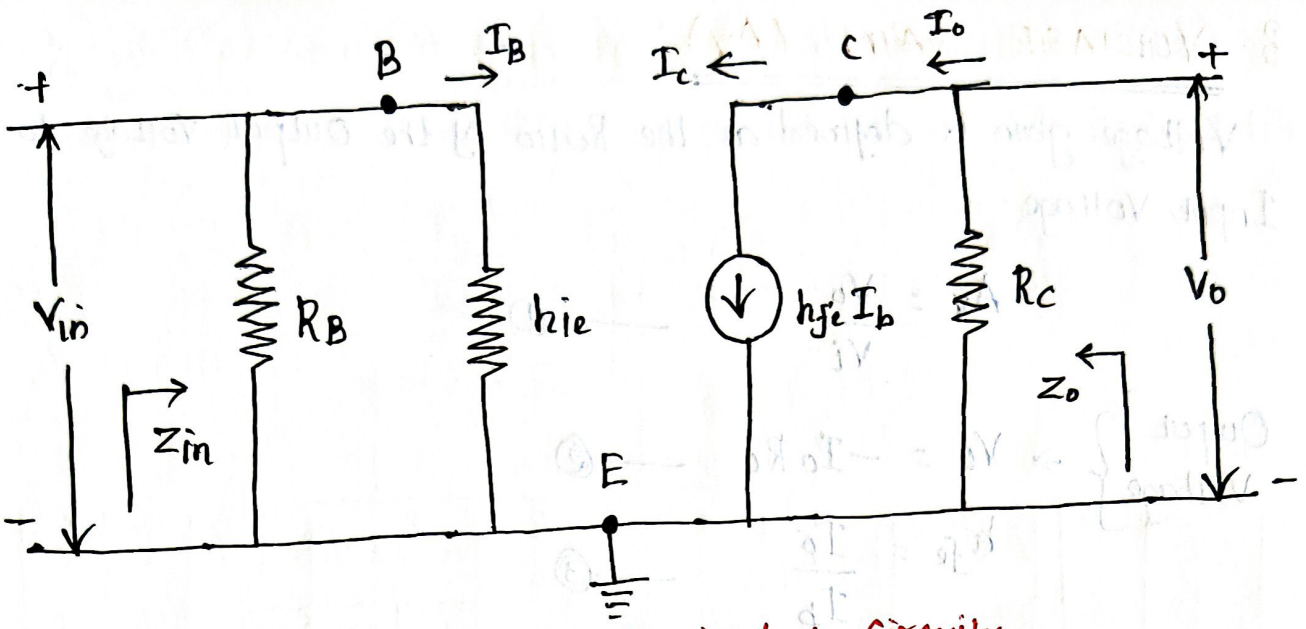


Fig. 3. Modified Hybrid Equivalent Circuit.

1. INPUT IMPEDANCE : (Z_i)

From the fig.3, the Input Impedance can be calculated as

$$Z_{in} = R_B \,||\, h_{ie}$$

$$Z_{in} = \frac{R_B \cdot h_{ie}}{R_B + h_{ie}}$$

If $R_B >> h_{ie}$, then

$$Z_i \simeq \frac{R_B h_{ie}}{R_B}$$

$$\boxed{Z_i \approx h_{ie}}$$

2. OUTPUT IMPEDANCE (Z_o)

It is defined as the Impedance determined with Input Voltage $V_i = 0$

From Fig.3, If $V_i = 0$, then $I_b = 0$

$$\Rightarrow h_{fe} I_b = 0.$$

Current Source is open circuited.

$$Z_o = R_L = R_C$$

$$\boxed{Z_o = R_C}$$

3. VOLTAGE GAIN (A_V)

Voltage gain is defined as the Ratio of the Output Voltage to Input Voltage.

$$A_V = \frac{V_o}{V_i} \quad \text{—— (1)}$$

Output Voltage $\rightarrow V_o = -I_o R_C$ —— (2)

$$h_{fe} = \frac{I_o}{I_b} \quad \text{—— (3)}$$

$$I_o = h_{fe} I_b \quad \text{—— (4)}$$

Substitute eqn (4) in (2)

$$\boxed{V_o = -h_{fe} I_b R_C} \qquad \boxed{V_o = -h_{fe} I_b R_C}$$

Input Voltage $\rightarrow V_i = I_b (R_B \| h_{ie})$

$$= I_b \left(\frac{R_B \cdot h_{ie}}{R_B + h_{ie}} \right)$$

Assume $R_B \gg h_{ie}$ and Neglecting h_{ie}.

$$V_i = I_b \frac{R_B h_{ie}}{R_B}$$

$$\boxed{V_i = I_b h_{ie}}$$

Hence $A_V = \frac{V_o}{V_i}$

$$= \frac{-h_{fe} I_b R_C}{I_b h_{ie}}$$

$$\boxed{A_V = \frac{-h_{fe} R_C}{I_b}}$$

The Negative sign implies that there is 180° phase shift between Input and Output Signals

4. CURRENT GAIN (A_I)

Current Gain is the Ratio of Output Current to Input Current

$$A_I = \frac{I_o}{I_i}$$

$$= \frac{-h_{fe} I_b}{I_b}$$

$$\boxed{A_I = -h_{fe}}$$

CE AMPLIFIER WITH EMITTER RESISTOR (R_E) AND BYPASS CAPACITANCE (C)

A common Emitter Amplifier Circuit is shown in fig. 4, the Circuit Consists of Biasing Resistors R_1 and R_2, the temperature Stabilization Resistor R_E, Collector Resistor R_C.

* The By Pass Capacitor 'C' is used to eliminate ac degeneration i.e, it bypass all Ac signal and increase the Output Gain.

- The coupling capacitor C_1 Connects the Signal Source with the Transistor Base 'B'. C_2 Couples external Load Resistor R_L to the Collector of Transistor 'C'.

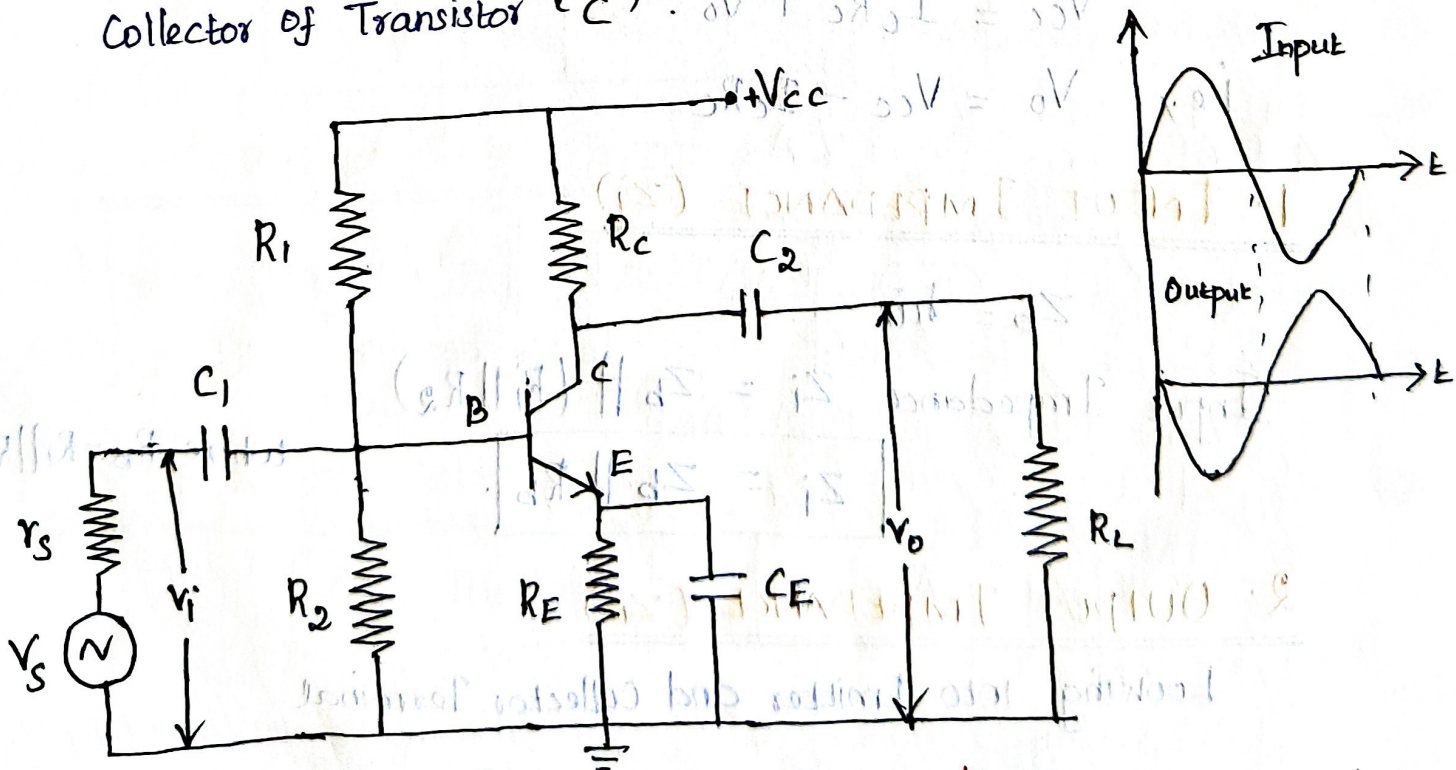


Fig. 4. Amplifier with Emitter Resistor.

- C_1 and C_2 avoids the loading effect between Input and Output.

OPERATION

When the Input Voltage is increased in positive direction, V_{BE} is increased. Thus Collector current 'I_c' increases, the Voltage drop occurs across R_c.

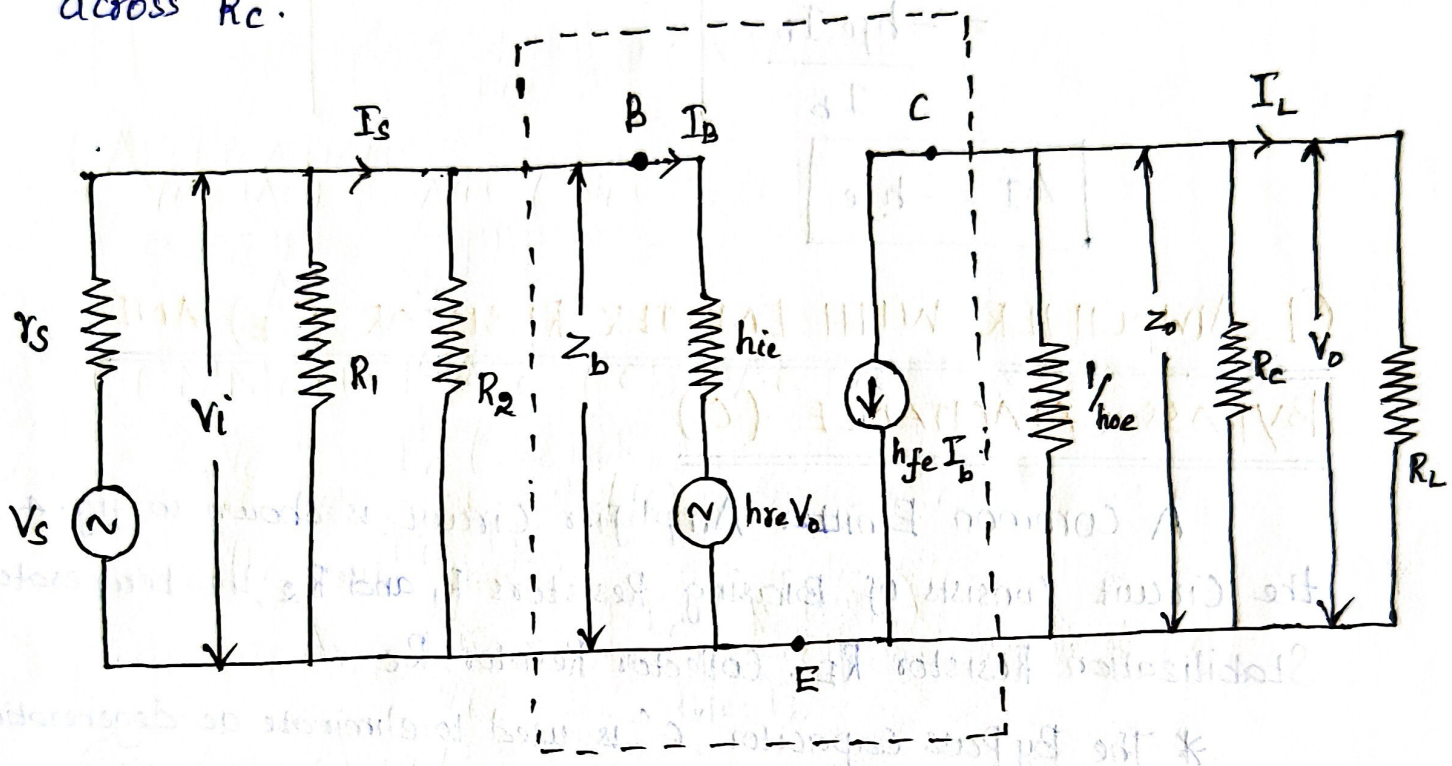


Fig.5. h-Parameter Model

Apply KVL to collector circuit

$$V_{CC} = I_C R_C + V_o$$

i.e., $$V_o = V_{CC} - I_C R_C$$

1. INPUT IMPEDANCE (Z_i)

$$Z_b = h_{ie}$$

Input Impedance $Z_i = Z_b \,||\, (R_1 \,||\, R_2)$

$$\boxed{Z_i = Z_b \,||\, R_b}$$

where, $R_b = R_1 \,||\, R_2$

2. OUTPUT IMPEDANCE (Z_o)

Looking into Emitter and collector Terminal

$$Z_c = \frac{1}{h_{oe}}$$

The Output Impedance is given by

$$Z_o = Z_c \,||\, R_c$$

$$\boxed{Z_o = \frac{1}{h_{oe}} \,||\, R_c}$$

3. VOLTAGE GAIN (A_v)

$$A_v = \frac{V_o}{V_i}$$

$$\therefore \quad V_o = -I_c (R_c || R_L)$$

$$\therefore \quad V_i = h_{ie} I_b$$

$$A_v = \frac{V_o}{V_i} = \frac{-I_c (R_c || R_L)}{h_{ie} I_b}$$

$$= \frac{-I_c}{I_b} \frac{(R_c || R_L)}{h_{ie}}$$

Where, $h_{fe} = \frac{I_c}{I_b}$.

$$\boxed{A_v = \frac{-h_{fe}}{h_{ie}} (R_c || R_L)}$$

4. CURRENT GAIN (A_I)

$$A_I = \frac{I_c}{I_s} \qquad \boxed{A_I = \frac{I_c}{I_s}}$$

5. POWER GAIN (A_p)

$$\boxed{A_p = A_v \cdot A_I}$$

Current divider Rule

$$I_B = \frac{R_B}{R_B + Z_B} I_s \quad -(1)$$

$$h_{fe} = \frac{I_c}{I_B} \quad \therefore I_c = I_B h_{fe} \quad -(2)$$

eqn (1) sub. in eqn (2)

$$I_c = \frac{h_{fe} I_s R_B}{R_B + Z_B} \quad -(3)$$

$$I_L = \frac{R_c}{R_c + R_L} I_c \quad -(4)$$

Sub (3) in (4)

$$I_L = \frac{h_{fe} I_s R_B R_c}{(R_B + Z_B)(R_c + R_L)}$$

$$A_I = \frac{I_L}{I_s} = \frac{h_{fe} R_B R_c}{(R_B + Z_B)(R_c + R_L)}$$

CHARACTERISTICS OF CE AMPLIFIER

1. Good Voltage Gain
2. Phase Inversion i.e, Output Voltage is 180° out of phase with Input
3. Good Current Gain and Power Gain
4. High Input and Output Impedance.

APPLICATIONS

1. Voltage Amplifier.

COMMON BASE (CB) AMPLIFIER ANALYSIS

The Base Terminal (B) is common between the Input and Output Circuit. The Input is applied to Emitter Terminal (E) and Output is taken from the Collector Terminal (C).

CONSTRUCTION

The Common Base Amplifier is shown in fig. 1. The potential divider Bias is applied through Resistors R_1 and R_2.

(c)

i) The Load Resistor R_L is connected to Transistor Collector Terminal

ii) The Signal Source is Coupled to the Transistor Emitter Terminal (E) through 'C_2'

iii) Capacitor 'C_1' Constitutes an Ac short circuit from the Base (B) terminal to Ground. So, all the Input Voltage appear across Base Emitter junction (BE)

iv) Capacitor 'C_3' acts as a Coupling Capacitor and it Prevents the Loading Effect due to R_C and R_L

OPERATION :

During positive half of Input Signal, the Emitter Terminal (E) is Positive and the Base (B) remains at a Constant Potential.

Therefore, a positive going signal reduces Base-Emitter Voltage (V_{BE}) which in turn reduces Collector current (I_C). Thus the Voltage drop across the Collector Resistor (R_C) also decreases.

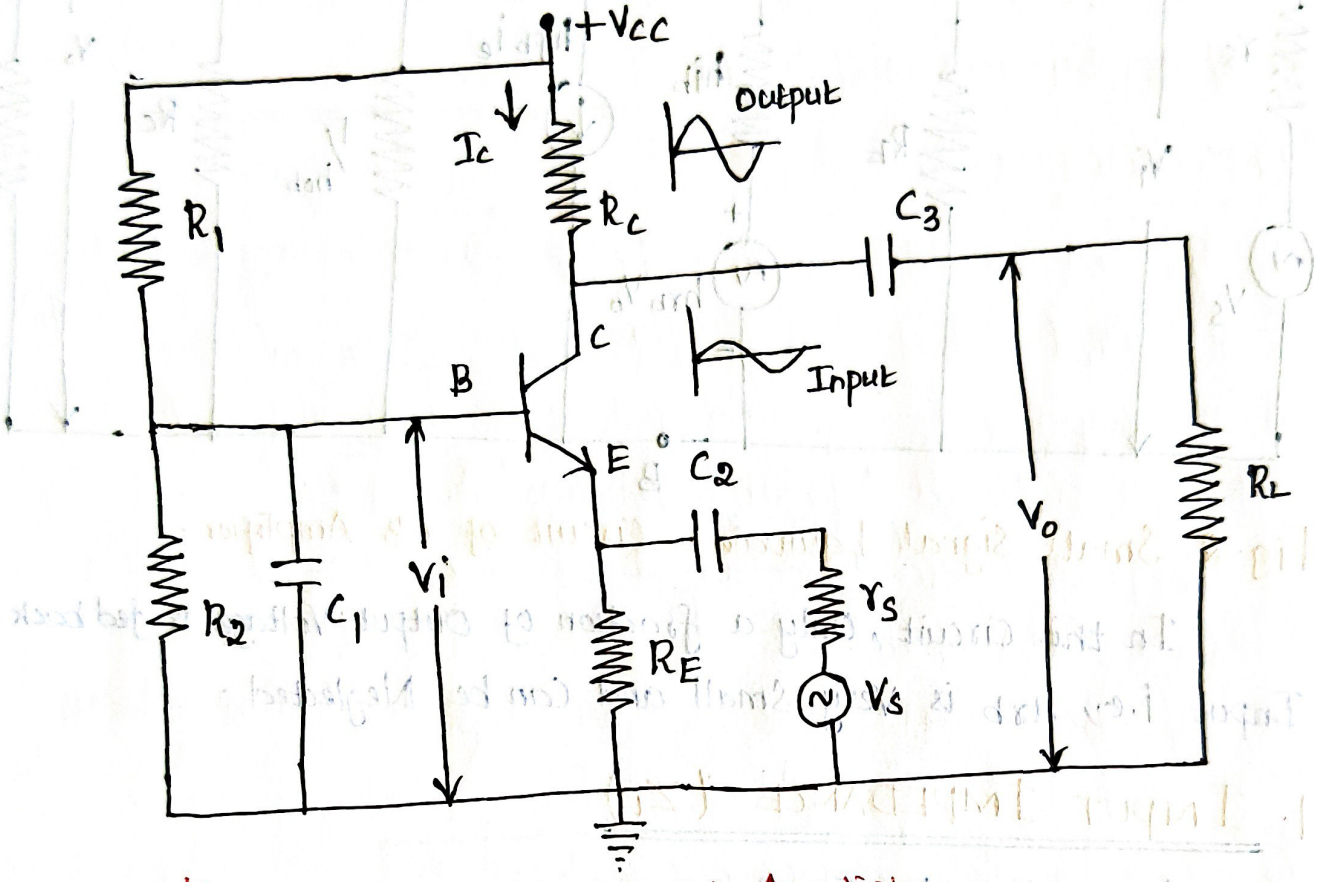


Fig.1. Common Base (CB) Amplifier

Apply KVL to the Output Circuit

$$V_{CC} = I_C R_C + V_o$$

$$\boxed{V_o = V_{CC} - I_C R_C}$$

If I_C reduces, then $V_o = V_{CC}$ and there is no phase shift between the Input and Output.

* During Negative Half cycle of Input, the Emitter Terminal (E) is Negative. Thus forward bias across Base-Emitter junction (BE) Increases which In-turn Increases the Collector current (I_C)

The Voltage drop across R_C Increases i.e., $I_C R_C > V_o$. Thus the Output Voltage ($V_o = V_{CC} I_C R_C$) decreases and the Output is Negative Value.

Fig.2 shows the Small Signal hybrid Equivalent of CB Amplifier

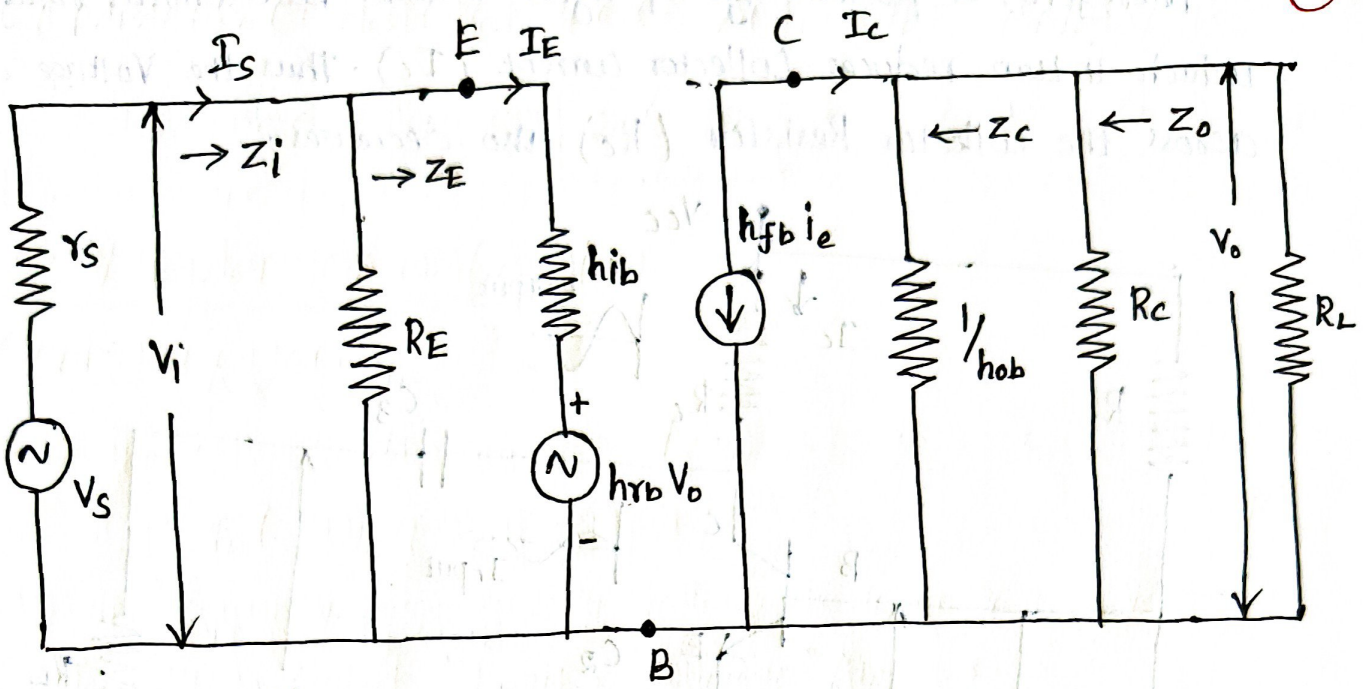


Fig. 2 Small Signal Equivalent Circuit of CB Amplifier.

In this circuit, only a fraction of output voltage is fed back to input i.e., h_{rb} is very small and can be neglected.

1. INPUT IMPEDANCE (Z_i)

Apply KVL to fig. 2

$$V_i = I_E h_{ib} + I_E R_B - I_C R_B \qquad (I_C = h_{fb} i_e)$$

$$V_i = I_E h_{ib} + I_E R_B - I_E h_{fb} R_B$$

$$\boxed{V_i = I_E [h_{ib} + R_B - h_{fb} R_B]}$$

$$Z_E = \frac{V_i}{I_E} = h_{ib} + R_B - h_{fb} R_B .$$

The Input Impedance can be written as

$$\boxed{Z_i = Z_E \,||\, R_E}$$

2. OUTPUT IMPEDANCE (Z_o)

$$Z_o = \frac{1}{h_{ob}}$$

The Output Impedance can be written as

$$Z_o = R_c \| z_c \simeq R_c$$

$$R_c << \frac{1}{h_{ob}} \quad \therefore \boxed{Z_o = R_c}$$

3. VOLTAGE GAIN (A_V)

$$A_V = \frac{V_o}{V_i}$$

$$V_o = I_c (R_c \| R_L)$$

$$V_i = I_E h_{ib}$$

$$\therefore A_V = \frac{V_o}{V_i} = \frac{I_c (R_c \| R_L)}{I_E h_{ib}} \qquad (R_B = R_1 \| R_2)$$

we know that $h_{fb} = \frac{I_c}{I_E}$

$$\boxed{A_V = \frac{h_{fb}}{h_{ib}} (R_c \| R_L)}$$

$h_{fb} = I_c / I_E$

Current divider Rule

$$I_L = \frac{R_E}{R_E + R_L} (I_c)$$

$$I_L = \frac{R_E}{R_E + R_L} (h_{fb} I_E)$$

$$I_E = \frac{R_B}{R_B + Z_E} (I_s)$$

Sub I_E in I_L

$$I_L = \frac{h_{fb} I_s R_B R_E}{(R_B + Z_E)(R_c + R_L)}$$

4. CURRENT GAIN (A_I)

$$\boxed{A_I = \frac{I_L}{I_s} = \frac{h_{fb} R_B R_E}{(R_B + Z_E)(R_c + R_L)}}$$

5. POWER GAIN (A_p)

$$\boxed{A_p = A_V \cdot A_I} \qquad A_p = A_V \cdot h_{fb}$$

CHARACTERISTICS OF CB AMPLIFIER

i) Provides Voltage Gain and Power Gain
ii) High Output Impedance and Very Low Input Impedance
iii) NO Current Gain

APPLICATION :

1. High Frequency Voltage Amplifier

COMMON COLLECTOR (CC) AMPLIFIER ANALYSIS

The Collector terminal is common between the input and output terminals. The Input is applied at the Base (B) and the Output is taken across the Emitter Terminal (E)

CONSTRUCTION:

i) The Collector Base Junction (CB) acts as Input and Emitter-Base Junction (BE) acts as Output

ii) The output voltage exactly follows the input voltage variations. Hence, it is called 'Emitter Follower' Amplifier.

iii) The Load Resistor (R_L) and capacitor 'C_2' coupled to the Emitter terminal (E) of the transistor

iv) The circuit employs Emitter current Bias through the voltage divider Resistors R_1 and R_2.

v) The capacitor C_1 and C_2 acts as Input and Output coupling capacitors.

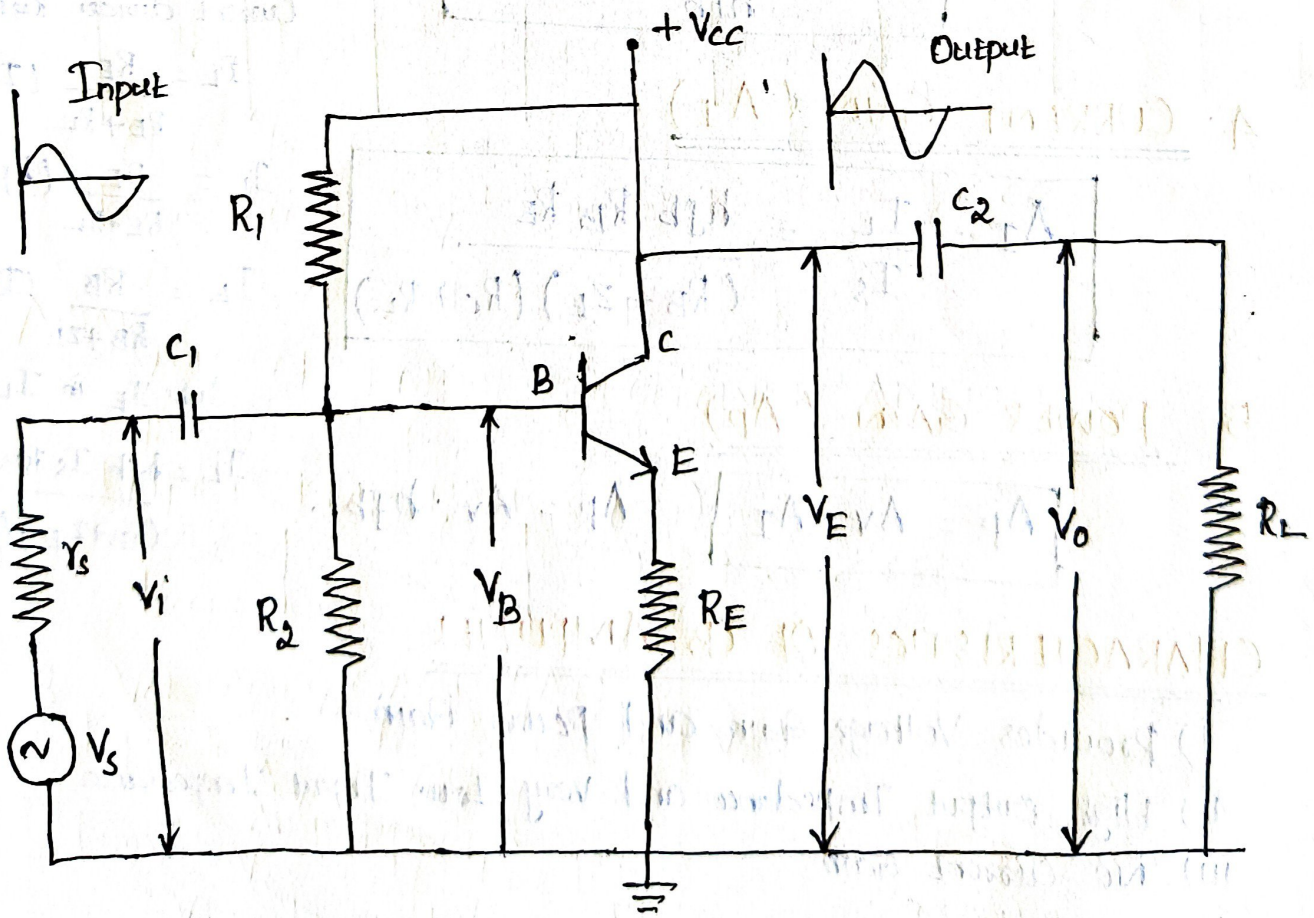


Fig. 1. Common Collector (CC) Amplifier.

OPERATION

When an Ac signal is applied to the Transistor Base (B) via 'C1', V_B is increased and decreased as the signal Varies from positive to Negative Voltage Variations.

$$V_E = V_B - V_{BE}$$

Thus the Output Voltage from a Common Collector Circuit is Same as its Input Voltage. So the 'CC Amplifier' has Unity Voltage Gain.

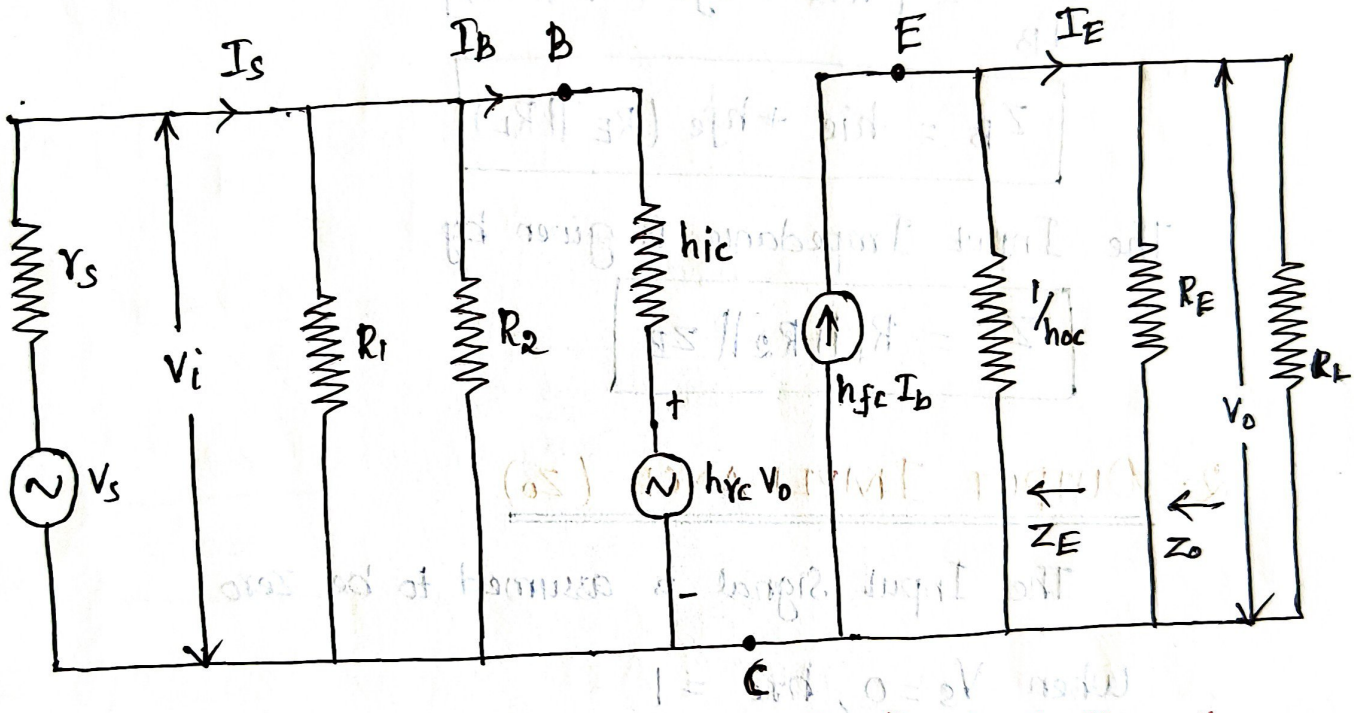


Fig.2. Small Signal Equivalent Circuit for CC configuration.

ANALYSIS OF EMITTER FOLLOWER AMPLIFIER

1. INPUT IMPEDANCE (Zi)

From fig.2, Applying KVL

$$V_o = I_E (R_E \| R_L) \quad \text{—— (1)}$$

Input Voltage, $V_i = I_B h_{ie} + V_o h_{re}$ —— (2)

For CC Amplifier, $h_{re} = 1$.

$$V_i = I_B h_{ie} + V_o = I_B h_{ie} + I_E (R_E \| R_L) \quad \text{—— (3)}$$

$$h_{fe} = \frac{I_E}{I_B}$$

$$\therefore I_E = I_B h_{fe} \quad \text{---} ④$$

Substitute eqn ④ in ③

$$V_i = I_B h_{ie} + h_{fe} I_B (R_E \| R_L)$$

$$= I_B [h_{ie} + h_{fe} (R_E \| R_L)]$$

$$\frac{V_i}{I_B} = [h_{ie} + h_{fe} (R_E \| R_L)]$$

$$\boxed{Z_B = h_{ie} + h_{fe} (R_E \| R_L)}$$

The Input Impedance is given by

$$\boxed{Z_i = R_1 \| R_2 \| Z_B}$$

2. OUTPUT IMPEDANCE (Z_o)

The Input Signal is assumed to be zero

When $V_s = 0$, $h_{re} = 1$

$$Z_E = \frac{V_o}{I_E} \quad ; I_E = h_{fc} I_B$$

The Output Impedance

$$Z_o = R_E \| Z_E$$

$$\boxed{Z_o = Z_E} \quad \text{if } R_E >> Z_E$$

3. VOLTAGE GAIN (A_V)

$$A_V = V_o / V_i$$

$$V_o = I_E (R_E \| R_L) \qquad I_E = h_{fc} I_B$$

$$V_o = h_{fc} I_b (R_E \| R_L) \quad \text{---} ①$$

Substitute $I_B = \frac{V_i - V_o}{h_{ic}}$ in eqn ①

$$V_o = \frac{h_{fc}\,(R_E \| R_L)}{h_{ic}}\,[V_i - V_o]$$

$$V_o = \frac{h_{fc}}{h_{ic}}(R_E \| R_L)\,V_i - \frac{h_{fc}}{h_{ic}}(R_E \| R_L)\,V_o.$$

$$V_o + \frac{h_{fc}}{h_{ic}}(R_E \| R_L)\,V_o = \frac{h_{fc}}{h_{ic}}(R_E \| R_L)\,V_i$$

$$V_o\left[1 + \frac{h_{fc}}{h_{ic}}(R_E \| R_L)\right] = \frac{h_{fc}}{h_{ic}}(R_E \| R_L)\,V_i$$

$$A_V = \frac{V_o}{V_i} = \frac{\frac{h_{fc}}{h_{ic}}(R_E \| R_L)}{1 + \frac{h_{fc}}{h_{ic}}(R_E \| R_L)}$$

$$\boxed{A_V \simeq 1}$$

4. CURRENT GAIN (A_I)

$$h_{fe} = \frac{I_E}{I_B}$$

$$R_B = R_1 \| R_2.$$

Applying Current division Rule

$$I_E = \frac{R_E}{R_E + R_L}(h_{fe} I_B) \quad \text{—①}$$

$$I_B = \frac{R_B}{R_B + Z_B}(I_S) \quad \text{—②}$$

Substitute ② in ① $I_E = \frac{h_{fe} I_S R_B R_E}{R_E + R_L}$

$$A_I = \frac{I_E}{I_S} = \frac{h_{fc} R_B R_E}{(R_E + R_L)(R_S + Z_B)}$$

$R_B >> Z_B$.

5. POWER GAIN (A_p)

$$A_p = A_V \cdot A_I$$

$A_V = 1$

$$A_p = A_V \cdot h_{fc}$$

$$\boxed{A_p = h_{fc}}$$

CHARACTERISTICS OF CC AMPLIFIER

1. Provides current Gain and power Gain
2. High Input Impedance and Very Low Output Impedance
3. No Voltage Gain.

APPLICATIONS

1. As Buffer Amplifier since Voltage Gain is Unity.
2. Impedance Matching Network.

COMPARISION OF CE, CB AND CC AMPLIFIERS.

S/No	CHARACTERISTICS	CE	CB	CC
1.	Input Impedance (z_i)	Low	Very Low	High
2.	Output Impedance (z_o)	High	Very High	Low
3.	Input Current	I_B	I_E	I_B
4.	Output Current	I_C	I_C	I_E
5.	Amplification Factor	$\beta = \frac{I_C}{I_B}$	$\gamma = \frac{I_E}{I_B}$	$\alpha = \frac{I_C}{I_E}$
6.	Current Gain (A_I)	High	High	< 1
7.	Voltage Gain (A_V)	Medium	Low	High
8.	Applications	As Audio signal Voltage Amplifier	1. As Input stage of Multi stage Amplifier 2. High Frequency Voltage Amplifier	1. Impedance Matching 2. Buffer Amplifier

SMALL SIGNAL FET MODEL

The Small Signal FET Model is used to relate small changes in FET Current and Voltages about quiscent Operating Point.

* FET is Considered to be in Common Source Configuration (CS)

There are two - Small signal models.

1. Low Frequency FET Model
2. High Frequency FET Model.

SMALL SIGNAL LOW-FREQUENCY FET MODEL

Fig.1 Shows the small signal Low-frequency model of a FET. Gate to Source Junction (GS) is represented by an open circuit and Current (I) is not drawn by the Input terminal of FET.

* The Input Resistance (r) is very large in the range of 10^8 to $10^{10}\Omega$. Typical Value of Drain Resistance (r_d) are from 100 kΩ to 1 MΩ.

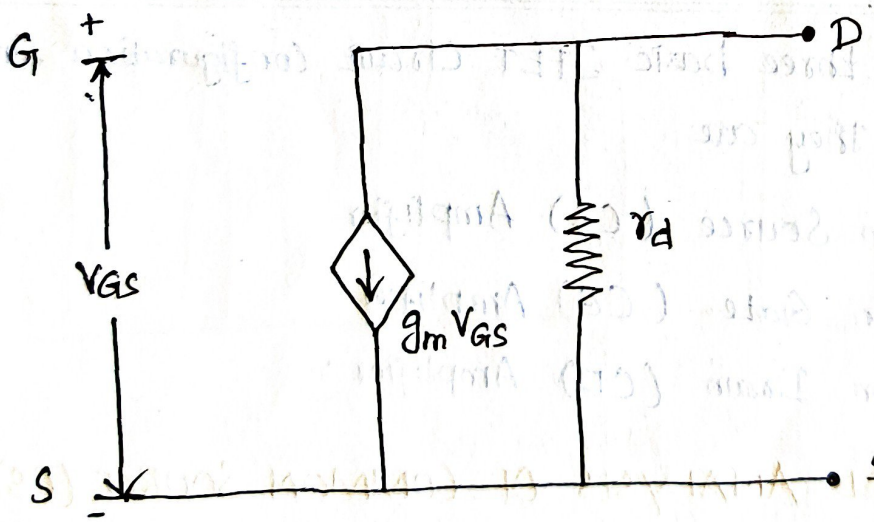


Fig. 1. Low-Frequency FET Model

SMALL SIGNAL HIGH-FREQUENCY FET MODEL

The high-frequency model is identical to the Low-frequency Model except that Capacitances are added between each pair of terminals.

- Fig. 2 shows the small signal High Frequency Model of FET. (G)

i) The capacitances 'C_{GS}' represents the Barrier capacitance between Gate and Source (S) Typical Values of 'C_{GS}' range from 1 PF to 10 PF.

ii) The capacitance 'C_{GD}' represents the Barrier capacitance between Gate (G) and Drain (D). Its typical value is also from 1 PF to 10 PF.

iii) The capacitance 'C_{DS}' represents the barrier capacitance between Drain (D) and Source (S). Its typical value range from 0.1 PF to 1 PF.

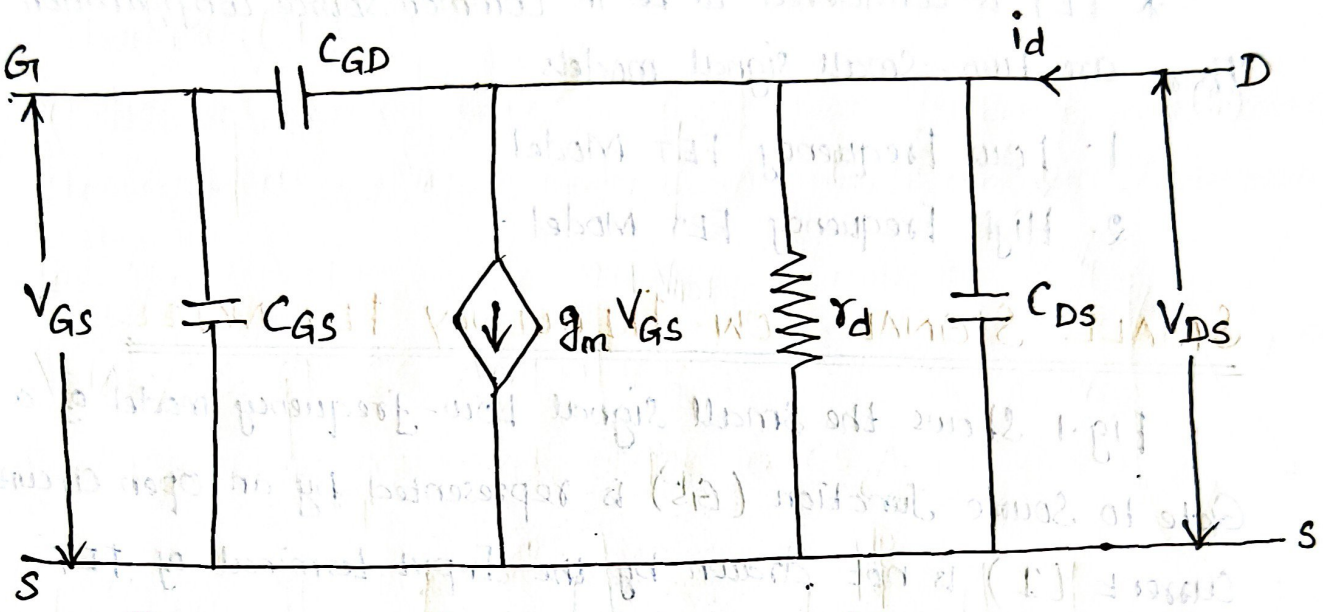


Fig: 2: High-Frequency FET Model

SMALL SIGNAL ANALYSIS OF JFET AMPLIFIERS

There are three basic JFET Circuit Configuration Similar to BJT Amplifiers. They are

1. Common Source (CS) Amplifier
2. Common Gate (CG) Amplifier
3. Common Drain (CD) Amplifier.

SMALL SIGNAL ANALYSIS OF COMMON SOURCE (CS) AMPLIFIER

The Small Signal Analysis of Common Source Amplifier is discussed in this Section.

CONSTRUCTION :

The Source Terminal (S) is common between Input and output Circuit. The Common Source Amplifier is shown in fig. 1

i) The Voltage divider Bias is applied through Resistors R_1 and R_2.

ii) Bypass capacitor `C2` is used to eliminate Ac degeneration. The Coupling capacitor `C1` connects the Input signal Source with the Gate Terminal (G)

iii) Capacitor `C3` Couples External Load Resistor `RL` to the Drain Terminal (D)

iv) Resistor Rs and Capacitor C_2 Provides Temperature Stabilization. The capacitor `C2` by pass all the Ac signals and avoid Ac degeneration.

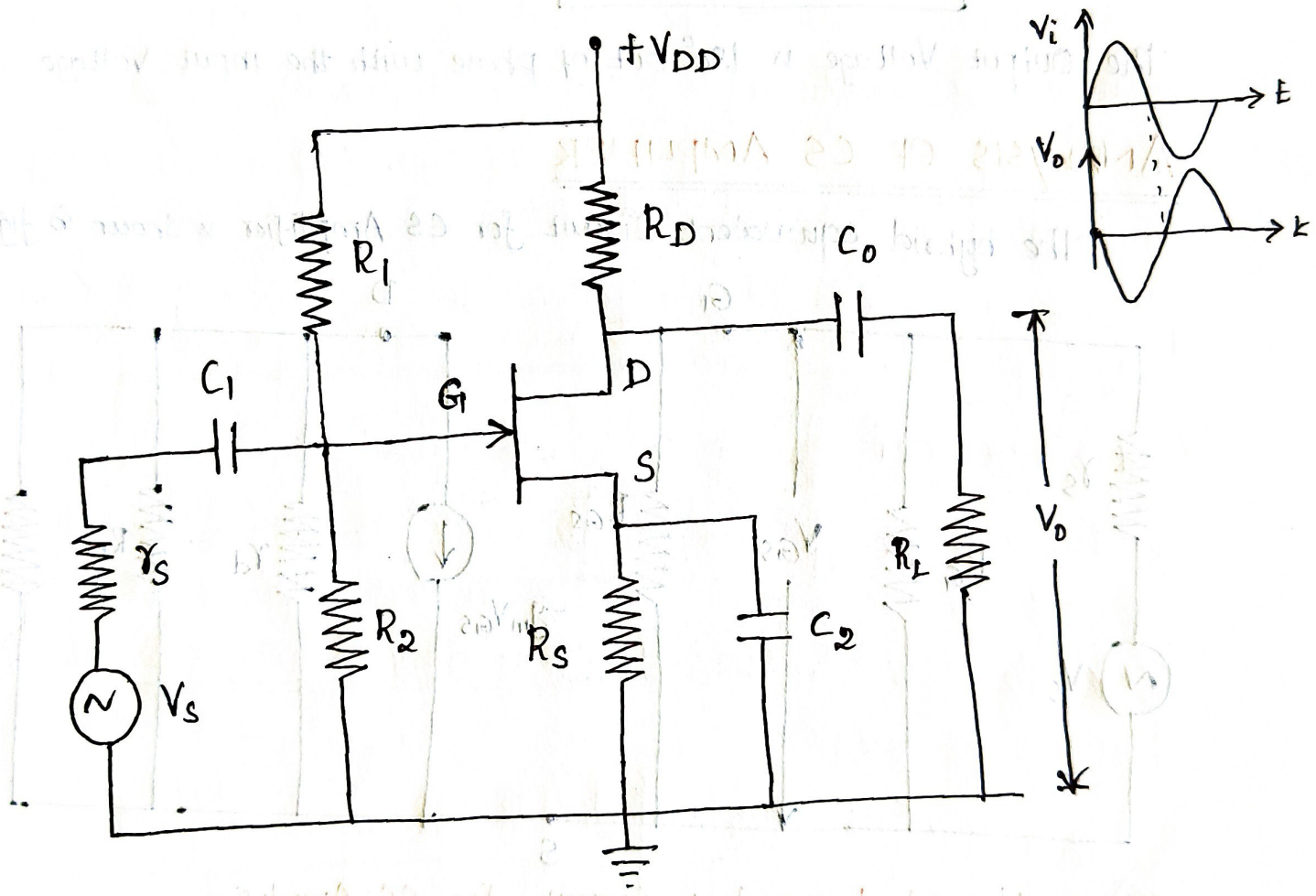


Fig.1. Common Source Amplifier.

OPERATION

i) Input Voltage is applied between the Gate Source Terminal (GS). When the Input Voltage Varies, the gate-Source Voltage (V_{GS}) Varies i.e., Biasing of Gate (G) and Source (S) makes drain Current (I_D) to increase and decrease accordingly.

ii) The change in `ID` changes the Voltage drop across Drain Resistor `RD` which produces Output Voltage `Vo`

iii) During positive half cycle of Input, Gate-Source terminal (GS) become less Reverse biased. This reduction in $-V_{GS}$ increases I_D

Apply KVL to the Output Circuit

$$V_{DD} = I_D R_D + V_D .$$

$$V_{DD} = I_D R_D + V_o$$

$$\boxed{V_o = V_{DD} - I_D R_D}$$

$I_D \uparrow \; V_D \downarrow$

The Output Voltage is 180° out of phase with the Input Voltage

ANALYSIS OF CS AMPLIFIER

The hybrid equivalent Circuit for CS Amplifier is shown in fig. 2

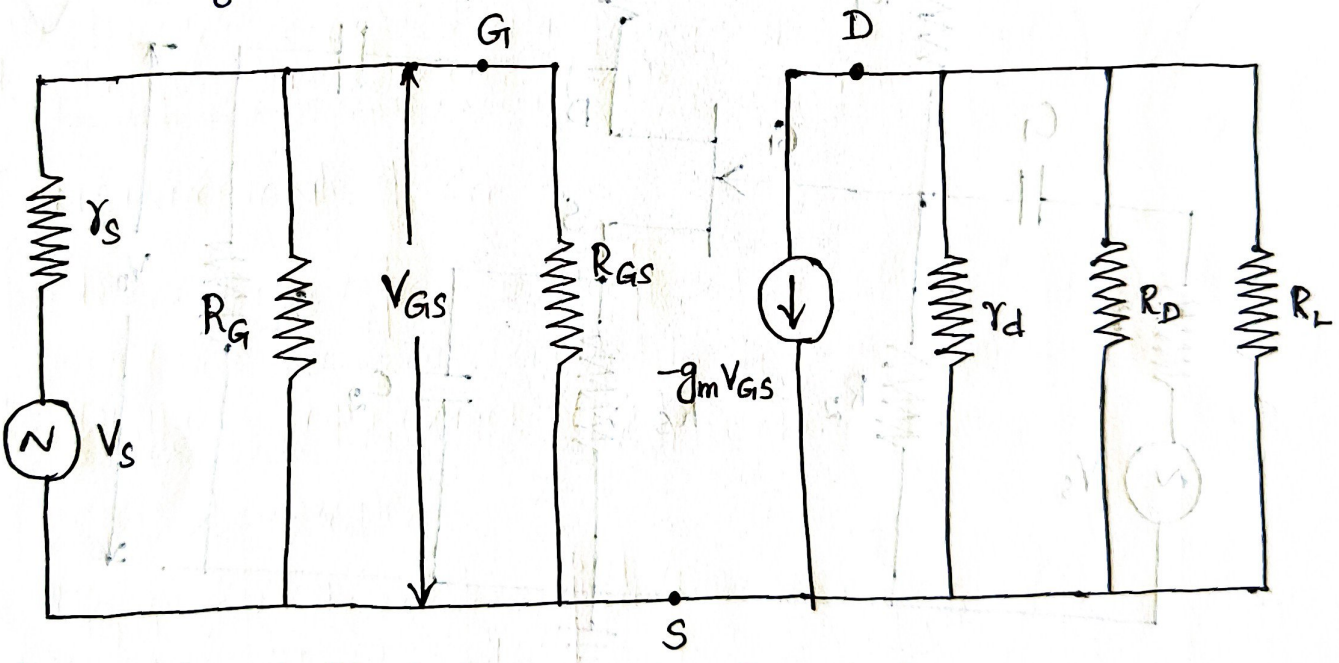


Fig. 2. Hybrid Equivalent Circuit for CS Amplifier.

The Input Impedance is given as

$$Z_G = R_{GS}$$

Apply KVL to Input Current

$$V_i = V_{GS} + I_D R_S \quad \text{—— (1)}$$

We know that, $V_{GS} = \dfrac{I_D}{g_m}$

$$I_D = V_{GS} g_m . \quad \text{—— (2)}$$

$$V_i = V_{GS} + g_m V_{GS} R_S$$

$$V_i = V_{GS} (1 + g_m R_S)$$

$$V_{GS} = \frac{V_i}{1 + g_m R_S}$$

$$I_i = \frac{V_{gs}}{R_{gs}} = \frac{V_i}{R_{gs}(1 + g_m R_S)}$$

$$\frac{V_i}{I_i} = R_{gs}(1 + g_m R_S)$$

where g_m - Transconductance

$$Z_g = \frac{V_i}{I_i} = R_{GS}(1 + g_m R_S)$$

1. INPUT IMPEDANCE (Z_i)

$$Z_i = R_G \| Z_G$$

If $Z_G >> R_G$ $\quad \boxed{Z_i \simeq R_G}$

2. OUTPUT IMPEDANCE (Z_o)

$$Z_d \simeq r_d$$

The Output Impedance of the circuit is given by

$$\boxed{Z_o = R_D \| Z_d}$$

3. VOLTAGE GAIN (A_V)

$$V_o = I_d (r_d \| R_D \| R_L)$$

$$I_d = -g_m V_i$$

$$V_i = -\frac{I_d}{g_m}$$

$$A_V = \frac{V_o}{V_i} = \frac{I_d (r_d \| R_D \| R_L)}{-I_d / g_m} = +g_m (r_d \| R_D \| R_L)$$

If $r_d >> R_D \| R_L$

$$A_V \simeq -g_m (R_D \| R_L)$$

Negative sign indicates that the Output Voltage is 180° out of phase with Input Voltage.

SMALL SIGNAL ANALYSIS OF COMMON DRAIN (CD) AMPLIFIER

The Drain Terminal (D) is made as Common Terminal (C) Between Input and Output Circuit.

i) The Input Signal is applied to the Gate (G) and the Output is taken from the Source (S)

ii) The Source (S) exactly follows the Input signal. So, this of amplifier is also known as "Source Follower"

CONSTRUCTION

The Output Voltage is developed across Resistor (R_S). The Load Resistor (R_L) is Capacitor Coupled to the Source Terminal (S) of the FET

* The Gate Bias Voltage (V_G) is obtained using potential divider Resistors R_1 and R_2.

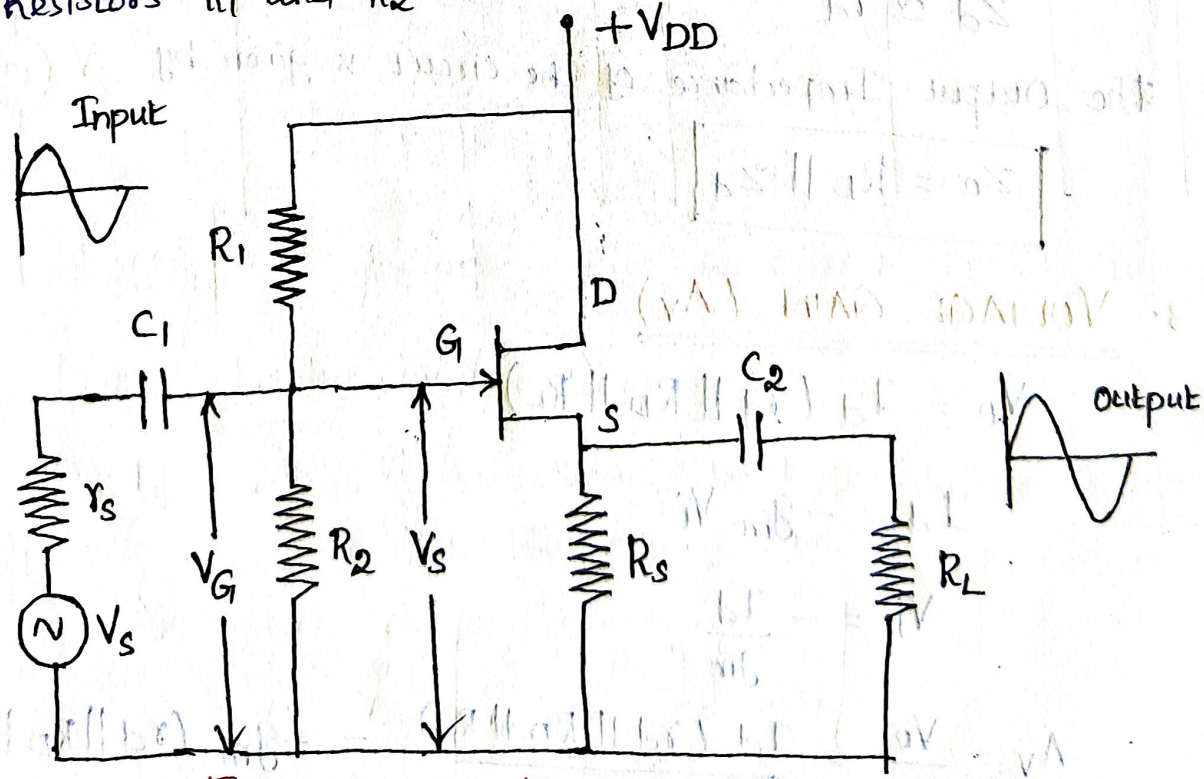


Fig. 1. Common Drain (CD) Amplifier.

OPERATION

i) When Input signal is applied to the FET Gate (G) via C_1, V_G is Increased and decreased as the input signal Varies from positive to Negative respectively. V_G is assumed to be constant.

$$V_S = V_G - V_{GS}$$

ii) The Output Voltage V_S increases when V_i increases and similarly the Output Voltage decreases when the input Voltage decreases.

iii) Thus Common drain Circuit has Unity Voltage Gain. So it is called 'Source Follower'.

ANALYSIS OF CD AMPLIFIER

Fig.2 shows the small signal equivalent Circuit for Common drain Amplifier.

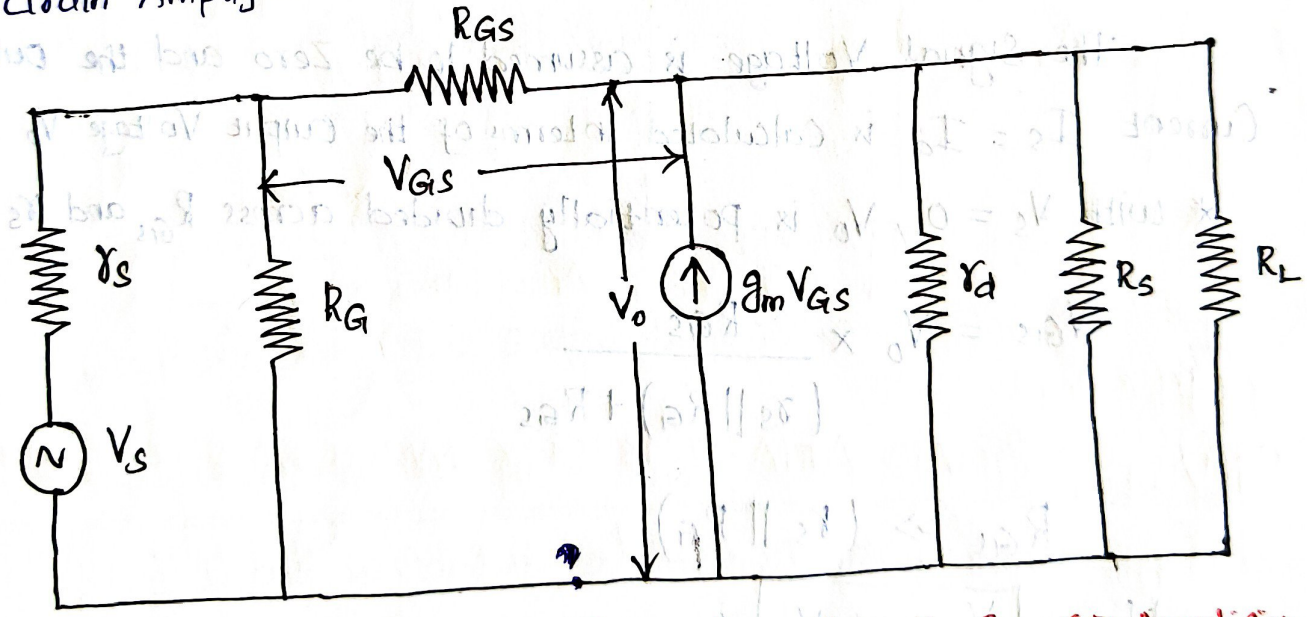


Fig.2. Small signal Ac Equivalent Circuit for CD Amplifier.

1. INPUT IMPEDANCE (Zi)

In Common drain Circuit, the External Load Resistor R_L appears in parallel with R_S

Apply KVL to the input Circuit

$$V_i = V_{GS} + V_o$$

V_o Can be written as

$$V_o = I_s (r_d \| R_s \| R_L)$$
$$\simeq I_d (r_d \| R_s \| R_L) \qquad (r_d >> R_s \| R_L)$$
$$= g_m V_{GS} (R_s \| R_L) \qquad V_{GS} = \frac{I_d}{g_m}$$

W.K.T $Z_g = \frac{V_{GS}}{I_g}$

Z_g = the Circuit Input Impedance is $R_G \| Z_g$

$$Z_i = R_G \| Z_g .$$

$$\boxed{Z_i \simeq R_G}$$

2. OUTPUT IMPEDANCE (Z_o)

- The Signal Voltage is assumed to be Zero and the Output Current $I_s = I_d$ is Calculated in terms of the Output Voltage V_o.

* with $V_s = 0$, V_o is potentially divided across R_{GS} and $r_s \| R_G$.

$$V_{GS} = V_o \times \frac{R_{GS}}{(r_s \| R_G) + R_{GS}}$$

$$R_{GS} >> (r_s \| R_G)$$

Hence $\boxed{V_{GS} \simeq V_o}$

$$I_d = g_m V_{GS}$$

$$Z_s = \frac{V_o}{I_d} = \frac{V_{GS}}{g_m V_{GS}} = \frac{1}{g_m}$$

Output Impedance $\boxed{Z_o = R_s \| \left(\frac{1}{g_m}\right)}$

3. VOLTAGE GAIN (A_V)

from figure-2

$$V_o = I_s (r_d \| R_s \| R_L)$$

$I_d = g_m V_{GS} = I_s$. Substitute I_s value in V_o

$$\therefore V_o = g_m V_{GS} (r_d \| R_s \| R_L)$$

$$V_i = V_{GS} + V_o = V_{GS} + g_m V_{GS} (r_d \| R_s \| R_L)$$

$$V_i = V_{GS} [1 + g_m (r_d \| R_s \| R_L)]$$

$$A_V = \frac{V_o}{V_i} = \frac{g_m V_{GS} (r_d \| R_s \| R_L)}{V_{GS} [1 + g_m (r_d \| R_s \| R_L)]}$$

$$A_V = \frac{g_m (R_s \| R_L)}{1 + g_m (R_s \| R_L)} \qquad \therefore (r_d >> R_s \| R_L)$$

$$\boxed{A_V \simeq 1} \quad \text{If } g_m (R_s \| R_L) >> 1$$

$A_V \simeq 1$ indicates that Output Voltage exactly follows the input signal

SMALL SIGNAL ANALYSIS OF COMMON GATE (CG) AMPLIFIER

The Input is applied to Source Terminal (S) and Output is taken from Drain Terminal (D) of JFET

CONSTRUCTION

The Common Gate (CG) Amplifier is shown in fig. 1. R_1 and R_2 acts as a potential divider circuit and R_L is the Load Resistor coupled to drain Terminal (D) through 'C_3'

i) The Input Voltage is coupled to the Source terminal (S) via C_2. C_1 constitute an Ac short circuit from the Gate terminal (G) to Ground.

ii) Since the Gate (G) is Shorted to Ground, all of the Input Voltage at Source of FET is developed across the Gate-Source Terminal (GS)

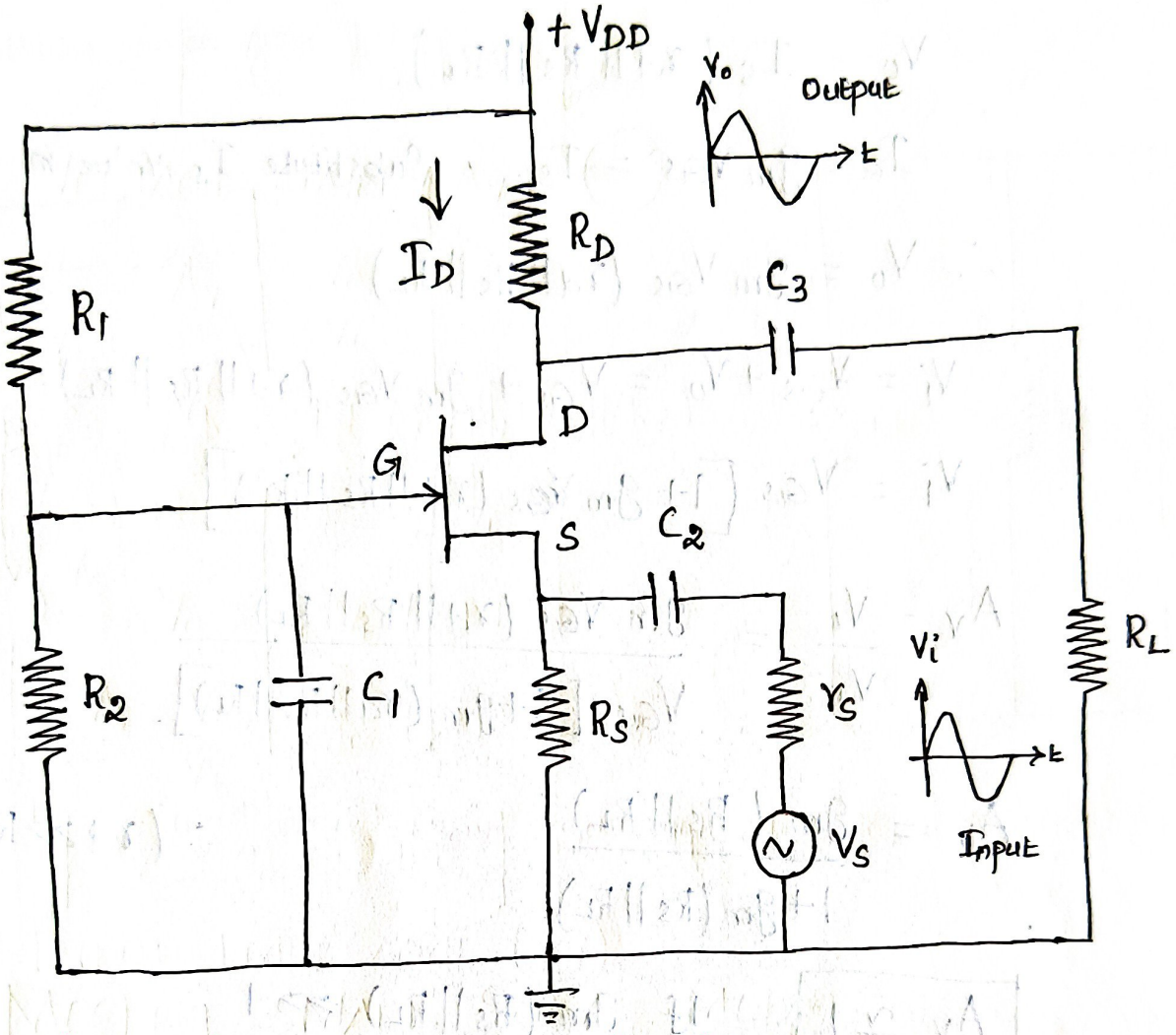


Fig. 1. Common Gate (CG) Amplifier

OPERATION :

When positive half signal is applied, the Source terminal (S) becomes positive and the Gate (G) remains at a constant potential.

ii) When an Input signal increases, Gate Source Voltage becomes Negative ($-V_{GS}$). This inturn reduces the drain Resistance (R_D).

$$V_D = V_{DD} - I_D R_D$$

Thus, If I_D reduces, V_D will increase i.e., the Positive going Input Produces a Positive-going output and Similarly the Negative half cycle of the Input results in Negative-going Output.

iii) There is No phase shift between Input and Output in the CG Amplifier.

ANALYSIS OF CG AMPLIFIER

Figure. 2 shows the small signal Hybrid Equivalent Circuit for Common Gate Amplifier.

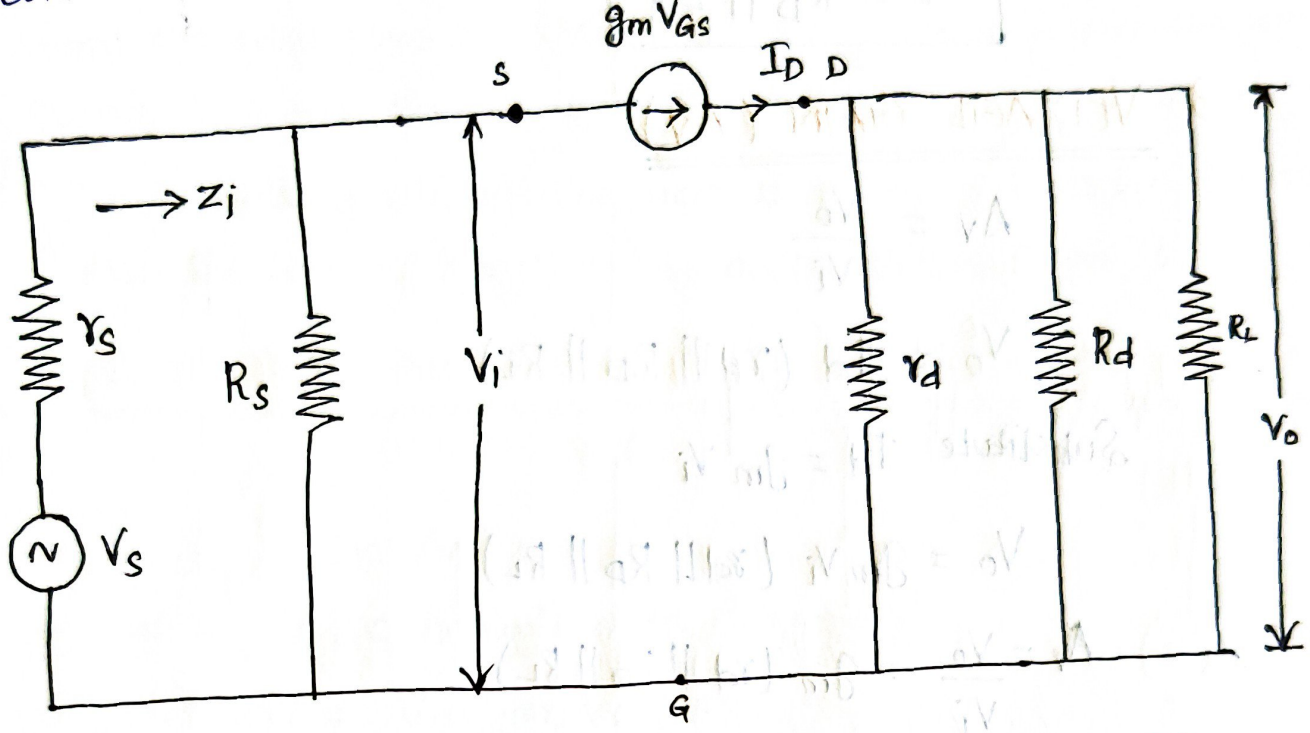


Fig. 2. Small signal hybrid equivalent Circuit for CG Amplifier

1. INPUT IMPEDANCE (Zi)

The Impedance between the Source (S) and Gate (G) terminals of the Common Gate Circuit is derived as follows.

$$V_i \simeq V_{GS}$$

$$I_D = g_m V_{GS}$$

$$Z_S = \frac{V_{GS}}{I_D} = \frac{V_{GS}}{g_m V_{GS}} = \frac{1}{g_m}$$

The Circuit Input Impedance is

$$\boxed{Z_i = R_S \,||\, Z_S = R_S \,||\, \frac{1}{g_m}}$$

2. OUTPUT IMPEDANCE

The Output of a CG Amplifier is taken from the drain Terminal (D).

The Output Impedance at the drain Terminal is

$$Z_d = r_d$$

$$\boxed{Z_o = R_D \,||\, Z_d}$$

3. VOLTAGE GAIN (A_V)

$$A_V = \frac{V_o}{V_i}$$

$$V_o = I_d \,(r_d \,||\, R_D \,||\, R_L)$$

Substitute $I_d = g_m V_i$

$$V_o = g_m V_i \,(r_d \,||\, R_D \,||\, R_L)$$

$$A_V = \frac{V_o}{V_i} = g_m \,(r_d \,||\, R_D \,||\, R_L)$$

$$\boxed{A_V \simeq g_m \,(R_D \,||\, R_L)} \qquad \text{if } r_d \gg R_D \,||\, R_L$$

MOSFET SMALL SIGNAL MODEL

The small signal model of MOSFET can be obtained similar to JFET. Figure.1 shows the small signal equivalent circuit of MOSFET.

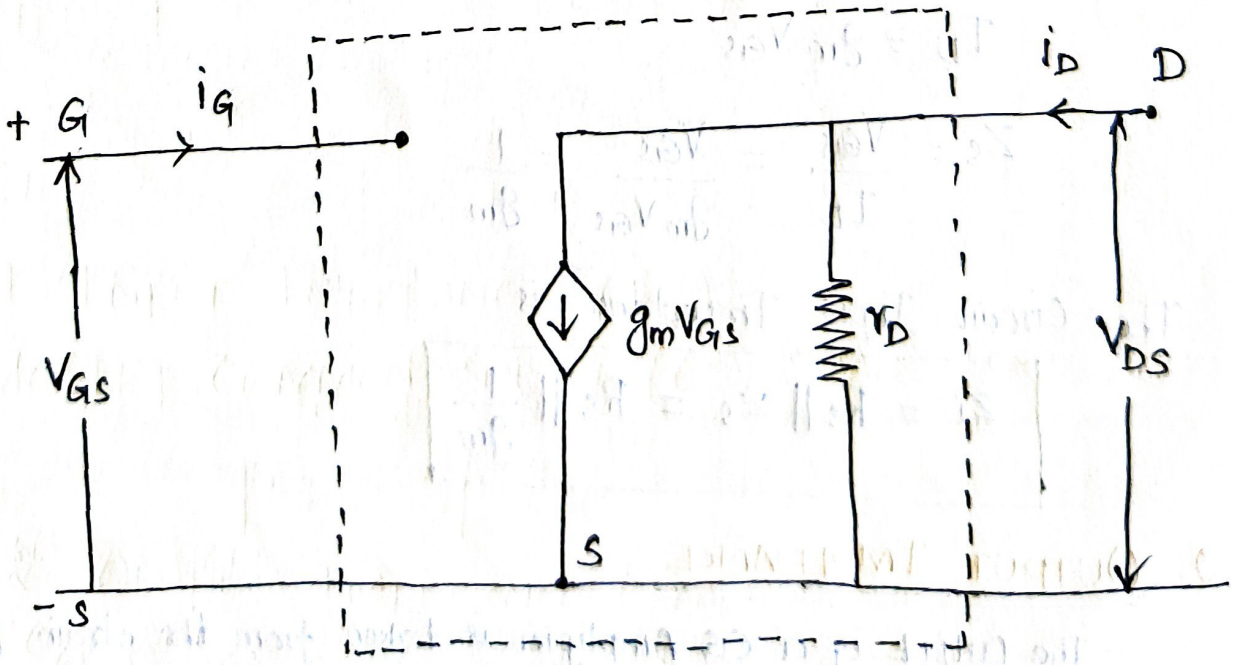


Fig.1. Small signal model of MOSFET

Since Gate (G) is insulated from channel by gate-oxide, Input Resistance of transistor is infinite

i) Small signal Parameters are controlled by the Q-point. For the same operating point, MOSFET has lower Transconductance and an Output Resistance that is similar to the BJT

ii) In Saturation mode, MOSFET acts as a Voltage Controlled Current Source. The Control voltage is V_{GS} an the Output Current is 'i_D'

STEPS INVOLVED IN SMALL-SIGNAL ANALYSIS OF MOSFET

STEP : 1

Complete a DC Analysis

The goal of this DC Analysis is to determine

a) the dc Voltage V_{GS} for MOSFET

b) the dc Voltage V_{DS} for MOSFET

STEP : 2

Calculate the Small signal circuit Parameters for the MOSFET

STEP : 3

Replace all MOSFETs with their Small-signal Circuit Model.

STEP : 4

Set all dc Sources to Zero

STEP : 5

Analyze Small signal Circuit.

MOSFET COMMON SOURCE (CS) SMALL SIGNAL AMPLIFIER

The common Source MOSFET amplifier is shown in figure. 1

CONSTRUCTION :

i) 'C_{C1} and C_{C2} are the Coupling capacitors and C_S is By pass capacitor

The Capacitance Values are Chosen to be large So that their reactances are Very Small at the operating Frequency.

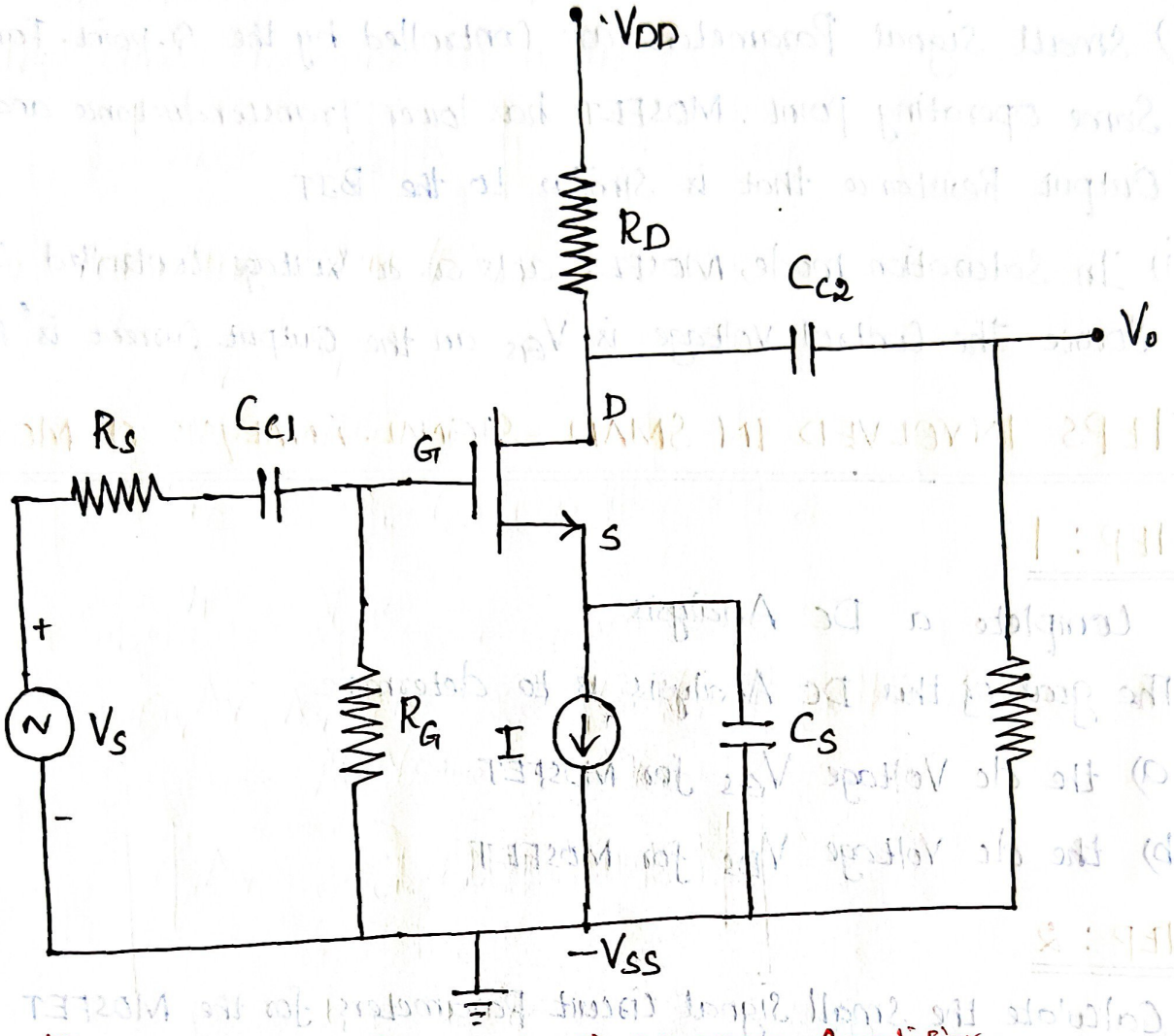


Fig.1: Common Source (CS) MOSFET Amplifier.

ANALYSIS

Fig.2 Shows the Small signal Equivalent Circuit for the Common Source MOSFET Amplifier.

- We will Calculate the input and Output Impedances, Current and Voltage gain Similar to BJT and FET

1. INPUT IMPEDANCE (R_{in})

From the fig.2, $I_g = 0$.

$$\boxed{R_{in} = R_G}$$

2. OUTPUT IMPEDANCE (R_{OUT})

To Calculate the Output Impedance, we get $V_s = 0$

When $V_s = 0 \Rightarrow g_m V_{GS} = 0$.

The Input Impedance of the dependent Current Source is infinite. Thus output Impedance is written as

$$\boxed{R_{out} = r_o \,||\, R_D}$$

3. VOLTAGE GAIN (A_V)

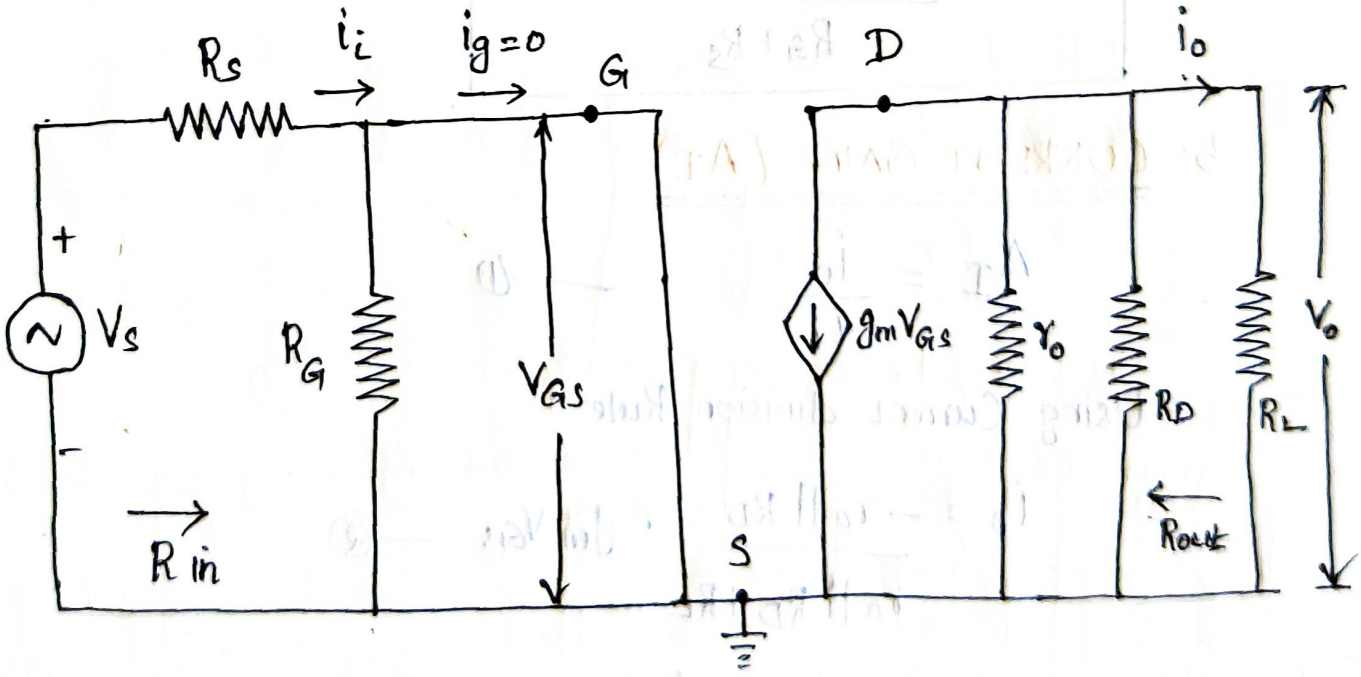
$$A_V = \frac{V_o}{V_i}$$

$$V_o = -g_m V_{GS} (r_o \,||\, R_D \,||\, R_L)$$

$$V_i = V_{GS}$$

$$\therefore \quad A_V = \frac{V_o}{V_i} = \frac{-g_m V_{GS} (r_o \,||\, R_D \,||\, R_L)}{V_{GS}}$$

$$\boxed{A_V = -g_m (r_o \,||\, R_D \,||\, R_L)}$$



Fig·2· Small signal Circuit for Common Source MOSFET

4. OVERALL VOLTAGE GAIN (G_V)

$$G_V = \frac{V_o}{V_s} = \frac{V_o}{V_i} \times \frac{V_i}{V_s} = A_V \frac{V_i}{V_s} \quad \text{——} (1)$$

Applying Voltage division Rule

$$V_i = \frac{R_{in}}{R_{in} + R_s} \cdot V_s \quad \text{——} (2)$$

Substitute $R_{in} = R_G$ from Input impedance

$$V_i = \frac{R_G}{R_{in} + R_s} V_s.$$

$$\frac{V_i}{V_s} = \frac{R_G}{R_{in} + R_s} \quad \text{——} (3)$$

Substitute eqn (3) in eqn (1)

$$G_V = A_V \cdot \frac{V_i}{V_s} = A_V \cdot \frac{R_G}{R_{in} + R_s} \quad \text{——} (4)$$

Substitute A_V value in (4)

$$\boxed{G_V = \frac{-g_m (r_o \| R_D \| R_L) \cdot R_G}{R_G + R_s}}$$

5. CURRENT GAIN (A_I)

$$A_I = \frac{i_o}{i_i} \quad \text{——} (1)$$

Using Current division Rule

$$i_o = \frac{-r_o \| R_D}{r_o \| R_D + R_L} \cdot g_m V_{GS} \quad \text{——} (2)$$

At the Input, $V_{GS} = i_i R_G$ —— (3)

Substitute (3) in (2)

$$i_o = \frac{-r_o \| R_D}{r_o \| R_D + R_L} \cdot g_m i_i R_G.$$

$$A_I = \frac{i_o}{i_i} = \frac{-r_o \,||\, R_D}{r_o \,||\, R_D + R_L} g_m R_G \quad \text{—④}$$

When $R_G \to \infty$, $A_V = \infty$

The equation ④ gives the overall current gain of CS Amplifier.

PROPERTIES

1. High Input Impedance
2. High Output Impedance.
3. Relatively High Small-signal Voltage Gain
4. Very High Small-signal Current Gain.

MOSFET COMMON DRAIN (CD) [SOURCE FOLLOWER] AMPLIFIER

The Input Signal is fed at the Gate (G) similar to the Common Source (CS) Amplifier. The signal Output is taken at the Source Terminal (S). The Source Follower using MOSFET is shown in figure. 1.

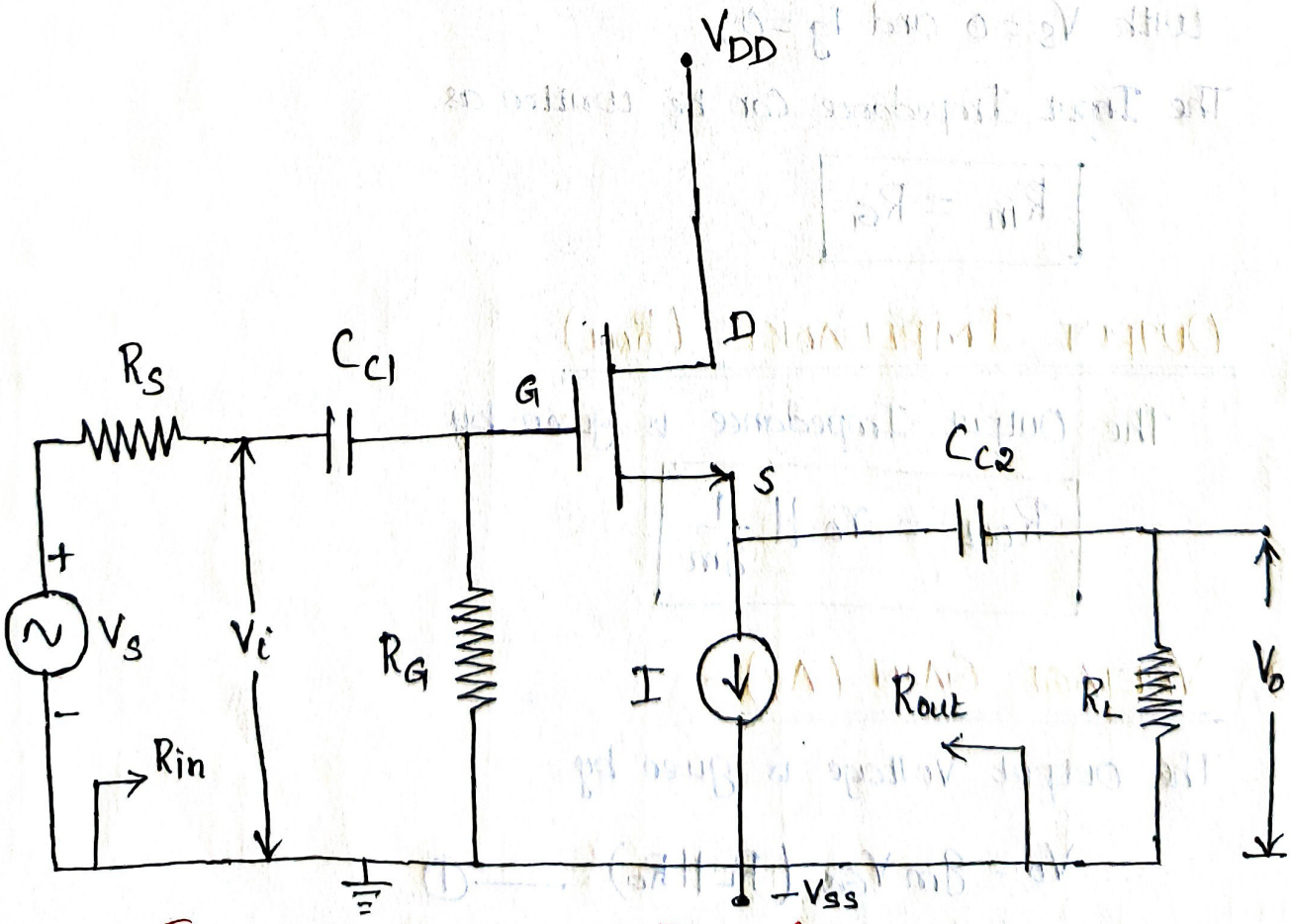


Fig. 1. MOSFET Common Drain Amplifier

The Small Signal Equivalent Circuit for Source follower MOSFET is shown in fig. 2.

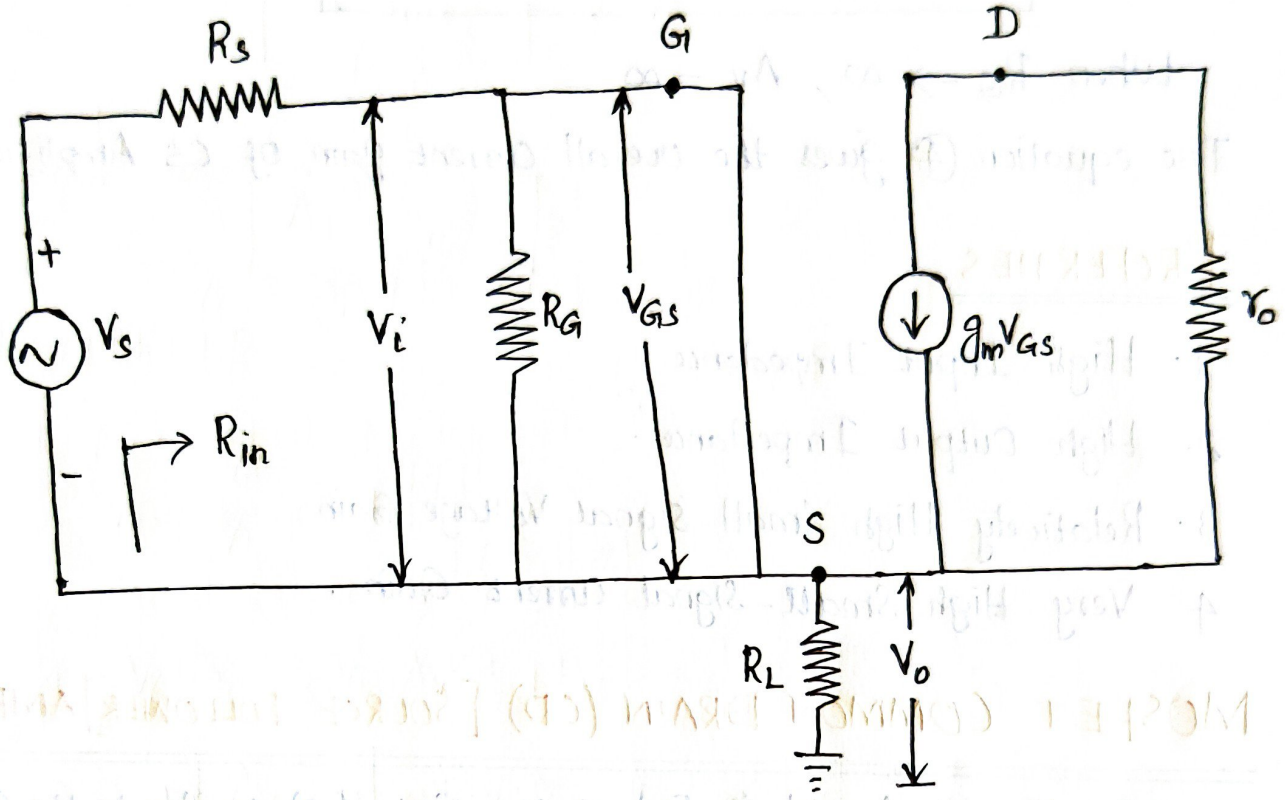


Fig. 2. Small Signal Equivalent Model of MOSFET Source follower

1. INPUT IMPEDANCE (R_{in})

With $V_s = 0$ and $i_g = 0$,

The Input Impedance can be written as

$$R_{in} = R_G$$

2. OUTPUT IMPEDANCE (R_{OUT})

The Output Impedance is given by

$$R_{OUT} = r_o \,||\, \frac{1}{g_m}$$

3. VOLTAGE GAIN (A_V)

The output Voltage is given by

$$V_o = g_m V_{GS} (R_L || R_o) \quad \text{---} (1)$$

The Input Voltage is obtained using Voltage division as

$$V_{gs} = \frac{\frac{1}{g_m}}{\frac{1}{g_m} + R_L \| r_o} \cdot V_i \quad \text{---} (2)$$

Substitute eqn (2) in eqn (1)

$$V_o = g_m (R_L \| R_o) \frac{\frac{1}{g_m}}{\frac{1}{g_m} + (R_L \| r_o)} V_i$$

$$A_V = \frac{V_o}{V_i} = \frac{R_L \| r_o}{\frac{1}{g_m} + (R_L \| r_o)}$$

If $r_o >> R_L$ and $R_L >> \frac{1}{g_m}$, then

$\boxed{A_V \simeq 1}$ Therefore it is called Source Follower.

4. CURRENT GAIN (A_I)

$$A_I = \frac{i_o}{i_i}$$

Let $i_g = 0$, Using Current division Rule

$$i_o = \frac{r_o}{r_o + R_L} g_m V_{gs}$$

Input Current, $i_i = \frac{V_i}{R_G}$

$$i_i = \frac{1 + g_m (R_L \| r_o)}{R_G} V_{gs}$$

$$A_I = \frac{i_o}{i_i} = \frac{\frac{r_o}{r_o + R_L} g_m V_{gs}}{\frac{1 + g_m (R_L \| r_o)}{R_G} V_{gs}} = \frac{r_o}{r_o + R_L} \frac{g_m R_G}{1 + g_m (R_L \| r_o)}$$

If $r_o >> R_L$ and $g_m R_L >> 1$, then

$$A_I \simeq \frac{R_G}{R_L}$$

If $R_L = 0$, then

$$A_I = g_m R_G$$

PROPERTIES

1. Non-Inverting Amplifier
2. Very Large Input Impedance
3. Small Output Impedance
4. Voltage Gain $A_V \leq 1$

HIGH FREQUENCY ANALYSIS

GAIN AND FREQUENCY RESPONSE OF BJT AMPLIFIER

Fig. 1 shows the high Frequency equivalent Circuit of CE Amplifier. All the Coupling and Bypass Capacitors have been assumed to be Short Circuited and wiring Capacitance is ignored

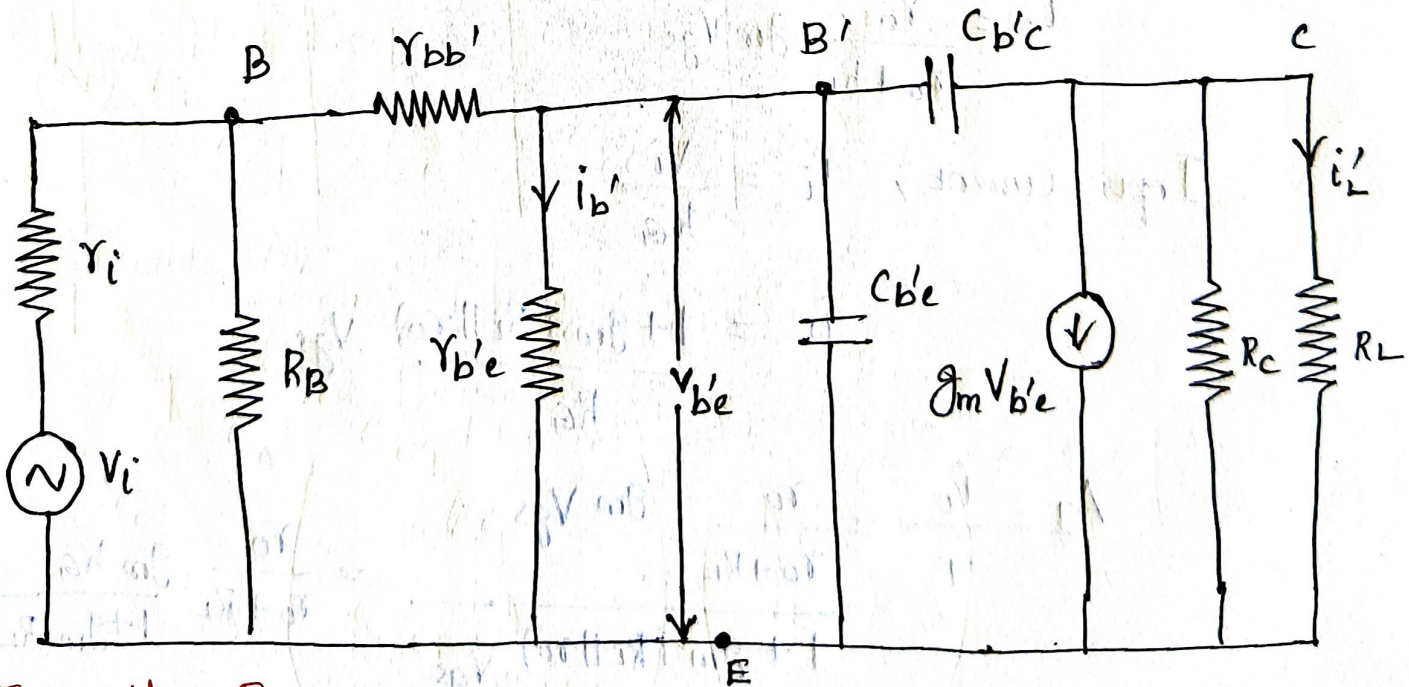


Fig. 1. High Frequency Equivalent Circuit of CE Amplifier.

Let $r_{b'c} \simeq h_{ie}$, $g_m V_{b'e} = h_{fe} I_b$ and $g_m = \frac{h_{fe}}{h_{ie}}$.

The fig.2 can be simplified using Millers theorem as follows

$$R_{be} = r_{be} \| (R_B \| r_{bb})$$

$$R_o = R_c \| R_L$$

The Input and output Feedback Capacitance $C_{b'c}$ are replaced by the input and output Shunting Capacitances. Fig.2 shows the modified Circuit of CE Amplifier.

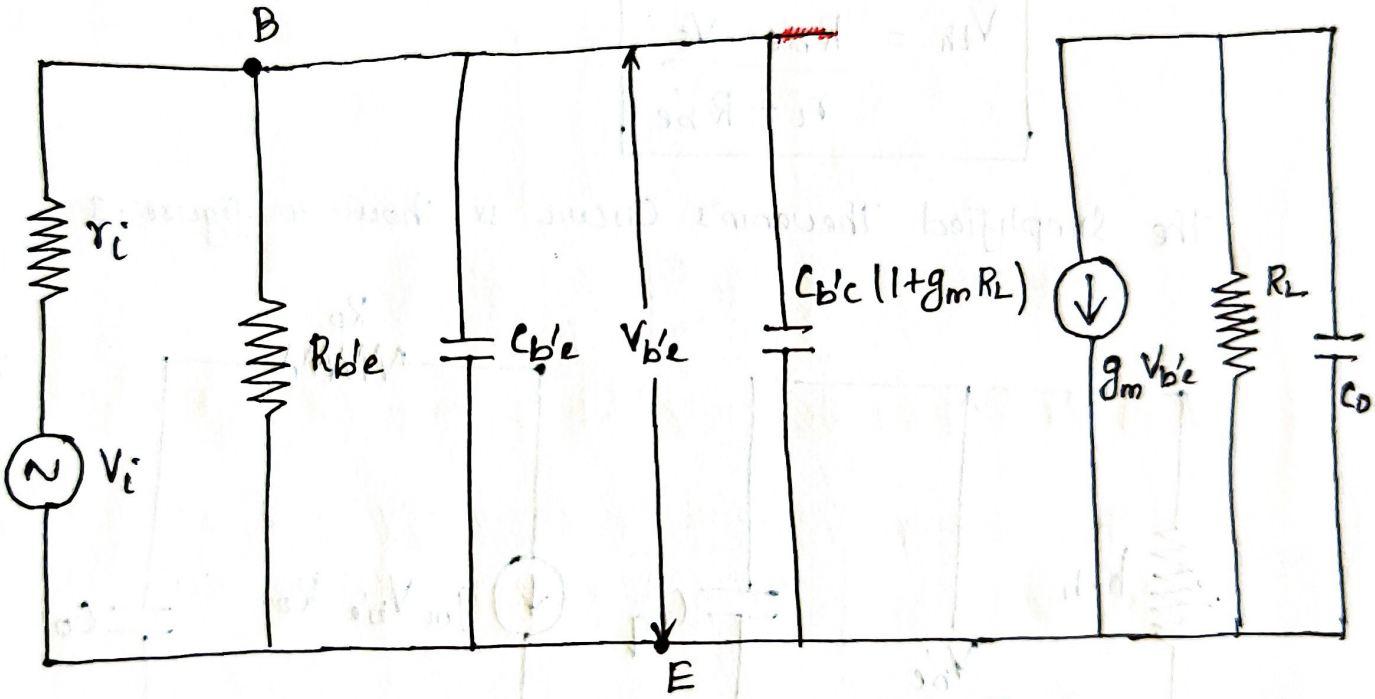


Fig.2. High Frequency Circuit using Miller's theorem

$$C_{eq} = C_{b'e} + C_{b'c}(1 + A_V)$$

Substitute $A_V = g_m R_L$

$$C_{eq} = C_{b'e} + C_{b'c}(1 + g_m R_L)$$

$$C_o = \frac{C_{b'c}(1+A_V)}{A_V} = \frac{C_{b'c}(1+g_m R_L)}{g_m R_L} = C_{b'c}\left(\frac{1}{g_m R_L} + \frac{g_m R_L}{g_m R_L}\right)$$

$$C_o = C_{b'c}\left(1 + \frac{1}{g_m R_L}\right)$$

Let us find the Thevenin's equivalent Circuit of the Input Circuit. The Thevenin's Impedance R_{th} is the Impedance looking from 'B' and E.

* To Calculate 'R_{th}', assume V_s to be Short Circuited and 'C_{eq}' is open Circuited. Then Thevenin's Voltage is measured as the Open Circuit Voltage measured across 'B' and 'E'

$$R_{th} = r_i \,||\, R_{b'e}$$

The Thevenin's Voltage is obtained as

$$V_{th} = \frac{R_{b'e} \cdot V_s}{r_i + R_{b'e}}$$

The Simplified Thevenin's Circuit is shown in figure: 3

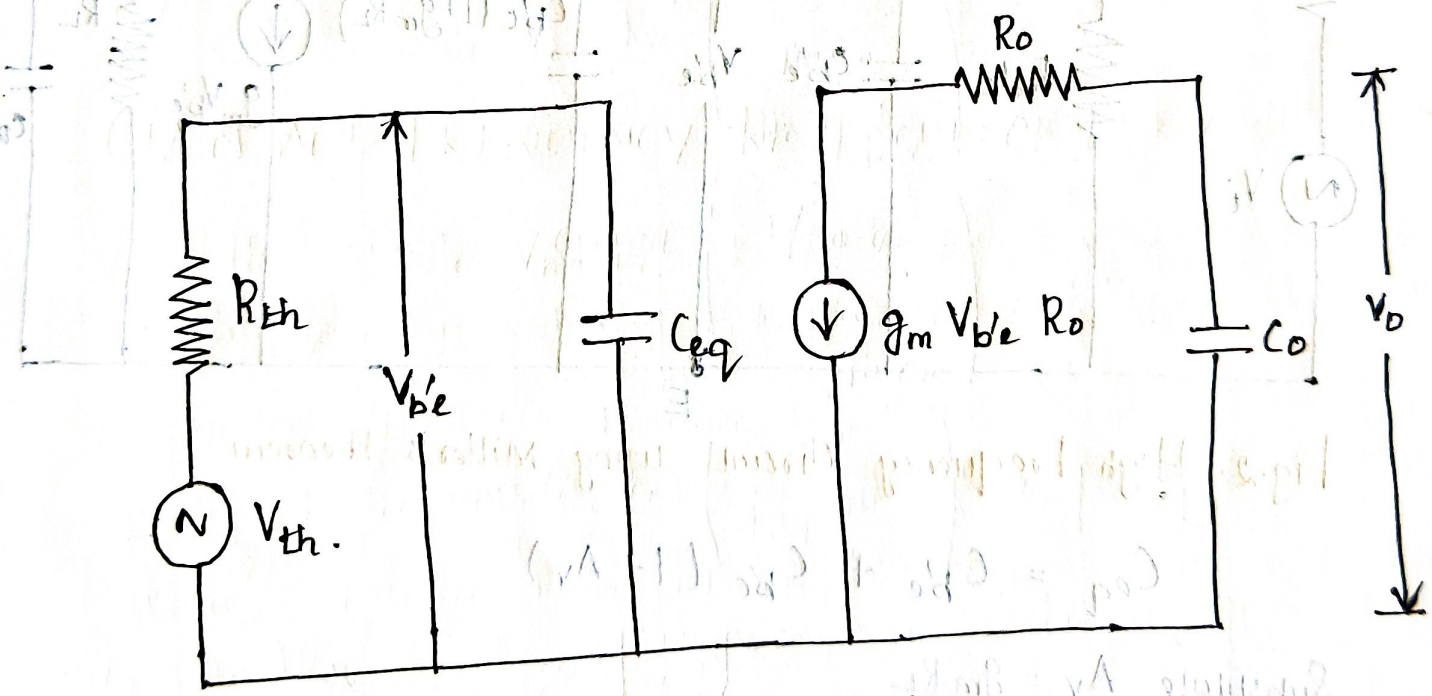


Fig. 3. Thevenin's Equivalent Circuit.

From the Thevenin's Equivalent Circuit.

$$V_{b'e} = \left(\frac{\frac{1}{j\omega C_{eq}}}{R_{th} + \frac{1}{j\omega C_{eq}}} \right) \left(\frac{R_{b'e} \cdot V_s}{r_i + R_{b'e}} \right)$$

$$V_{b'e} = \frac{1/j\omega C_{eq}}{\frac{R_{th}(j\omega C_{eq})+1}{j\omega C_{eq}}} \times \left(\frac{R_{b'e}}{r_i + R_{b'e}}\right) V_s .$$

$$= \frac{1}{1 + R_{th} j\omega C_{eq}} \left(\frac{R_{b'e}}{r_i + R_{b'e}}\right) V_s .$$

$$= \frac{1}{1 + j\left(\frac{\omega}{\omega_{21}}\right)} \left(\frac{R_{b'e}}{r_i + R_{b'e}}\right) V_s \quad \text{—— (1)}$$

where, $\omega_{21} = \frac{1}{R_{th} C_{eq}}$ = upper 3 dB cut off Frequency of input circuit.

Consider the Output Circuit,

$$V_o = -g_m V_{b'e} R_o \left(\frac{\frac{1}{j\omega C_o}}{R_o + \frac{1}{j\omega C_o}}\right)$$

$$= -g_m V_{b'e} R_o \left(\frac{1/j\omega C_o}{\frac{R_o j\omega C_o + 1}{j\omega C_o}}\right) = -g_m V_{b'e} R_o \left(\frac{1}{1 + R_o j\omega C_o}\right)$$

$$= -g_m V_{b'e} R_o \left(\frac{1}{1 + j\frac{\omega}{\omega_{22}}}\right) \quad \text{—— (2)}$$

where,

$\omega_{22} = \frac{1}{R_o C_o}$ = upper 3 dB cut off Frequency of output circuit.

We know that, Voltage Gain $A_V = \frac{V_o}{V_i}$

$$= \frac{V_o}{V_{b'e}} \cdot \frac{V_{b'e}}{V_i} \qquad V_s = V_i$$

Substitute (1) and (2)

$$= -g_m R_o \left(\frac{1}{1 + j\left(\frac{\omega}{\omega_{22}}\right)}\right) \frac{V_{b'e}}{V_{b'e}} \times \frac{1}{1 + j\left(\frac{\omega}{\omega_{21}}\right)} \left(\frac{R_{b'e}}{r_i + R_{b'e}}\right) \left(\frac{V_s}{V_i}\right)$$

$$= -g_m R_o \left(\frac{1}{1+j\left(\frac{\omega}{\omega_{22}}\right)}\right)\left(\frac{R_{b'e}}{r_i + R_{b'e}}\right) \times \left(\frac{1}{1+j\frac{\omega}{\omega_{21}}}\right)$$

Let $A_{vo1} = \dfrac{R_{b'e}}{r_i + R_{b'e}}$ = Mid Frequency Gain of Input Circuit.

$A_{vo2} = -g_m R_o$ = Mid Frequency Gain of Output Circuit.

Hence, A_v can be written as

$$A_v = A_{vo1} \cdot A_{vo2} \left(\frac{1}{1+j\frac{\omega}{\omega_{21}}}\right)\left(\frac{1}{1+j\left(\frac{\omega}{\omega_{22}}\right)}\right)$$

$$\boxed{A_v = A_{vo}\left(\frac{1}{1+j\frac{\omega}{\omega_{21}}}\right)\left(\frac{1}{1+j\left(\frac{\omega}{\omega_{22}}\right)}\right)}$$

This expression gives the Voltage Gain of the BJT Amplifier.

GAIN AND FREQUENCY RESPONSE OF FET AMPLIFIER

The equivalent circuit of FET Amplifier is shown in fig. 1. The Capacitors C_{gs} and C_{gd} in a JFET are due to Reverse biased Gate.

i) The Capacitance between the Source (S) and (G) C_{gs} is Similar to the Collector (C) Base (B) capacitance $[C_{b'e}]$ and the Capacitance between Drain (D) and Gate C_{ds} is Similar to Emitter (E) Base (B) capacitance $[C_{b'e}]$

The equivalent circuit can be modified using Miller's theorem as shown in fig. 2.

* The Input / Output Feedback capacitance C_{gd} is replaced by Input / Output shunting capacitance Similar to BJT Analysis.

Let $C_{mi} = C_{gd}(1 + A_v)$

$= C_{gd}\left[1 + g_m (r_s \| R_d)\right]$

$$C_{mo} = C_{gd}\left[1 + \frac{1}{g_m (r_{ds} \| R_d)}\right]$$

where,

$$A_v = g_m (r_{ds} \| R_D)$$

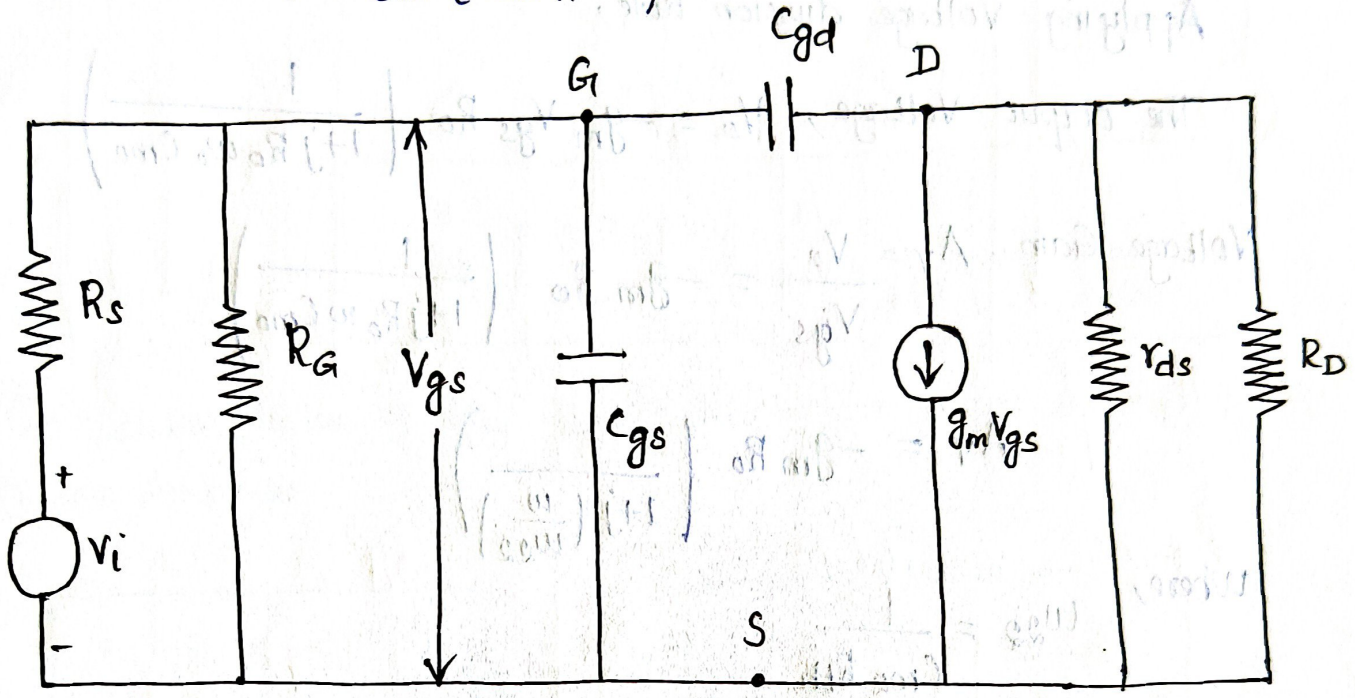


Figure 1. High Frequency Equivalent circuit of FET Amplifier

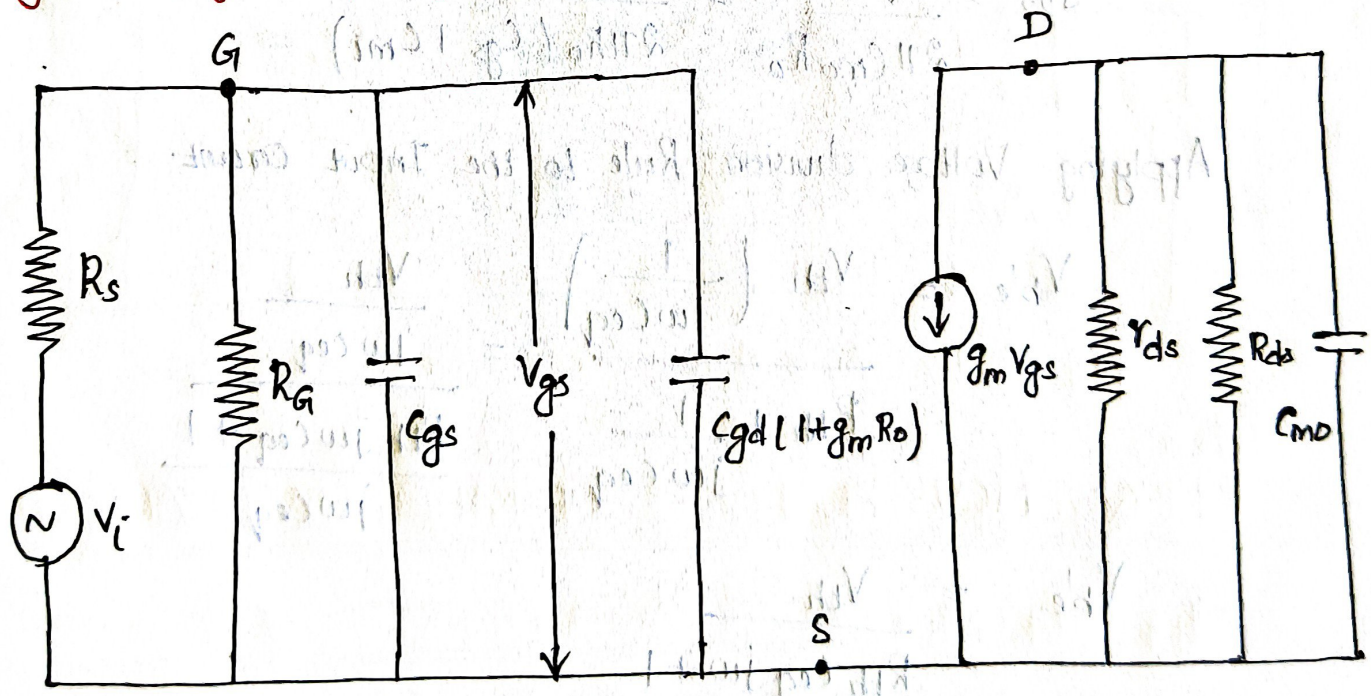


Fig. 2. Equivalent Circuit using Miler's Theorem.

The thevenin's Equivalent circuit for the above circuit is obtained as shown in fig. 3.

Thevenin's Impedance, $R_{th} = R_s \| R_G$

Thevenin's Voltage, $V_{th} \simeq V_s$

$$C_{eq} = C_{gs} + C_{gd}\,[1 + g_m (r_{ds} \| R_L)$$

$$R_o = r_{ds} \| R_D$$

Applying Voltage division Rule,

The output Voltage, $V_o = -g_m V_{gs} R_o \left(\frac{1}{1 + j R_o \omega_o C_{mo}} \right)$

Voltage Gain, $A_v = \frac{V_o}{V_{gs}} = -g_m R_o \left(\frac{1}{1 + j R_o \omega C_{mo}} \right)$

$$A_v = -g_m R_o \left(\frac{1}{1 + j \left(\frac{\omega}{\omega_{22}} \right)} \right)$$

Where, $\omega_{22} = \frac{1}{C_{mo} R_{Th}}$

$$f_{22} = \frac{1}{2\pi C_{mo} R_o} = \frac{1}{2\pi R_o (C_{gs} + C_{mi})}$$

Applying Voltage division Rule to the Input Circuit.

$$V_{b'e} = \frac{V_{Th} \left(\frac{1}{j\omega C_{eq}} \right)}{R_{Th} + \frac{1}{j\omega C_{eq}}} = \frac{\frac{V_{Th}}{j\omega C_{eq}}}{\frac{R_{Th}\, j\omega C_{eq} + 1}{j\omega C_{eq}}}$$

$$V_{b'e} = \frac{V_{Th}}{R_{Th} C_{eq} j\omega + 1}$$

$$V_{b'e} = \frac{V_{Th}}{1 + j \frac{\omega}{\omega_{21}}}$$

Where, $\omega_{21} = \frac{1}{R_{Th} C_{eq}}$ = upper 3dB Cut off Frequency due to Input Circuit.

Overall Voltage Gain, $V_o = \dfrac{-g_m R_o}{1+j\left(\frac{w}{w_{22}}\right)} V_{gs}$

$$= \frac{-g_m R_o}{1+j\left(\frac{w}{22}\right)} \quad \frac{V_{th}}{1+j\left(\frac{w}{w_{21}}\right)}$$

$$\boxed{\frac{V_o}{V_{th}} = -g_m R_o \left(\frac{1}{1+j\left(\frac{w}{w_{21}}\right)}\right)\left(\frac{1}{1+j\left(\frac{w}{w_{22}}\right)}\right)}$$

The Lowest Value of w_{21}, w_{22} is selected as upper 3 dB frequency of the Amplifier.

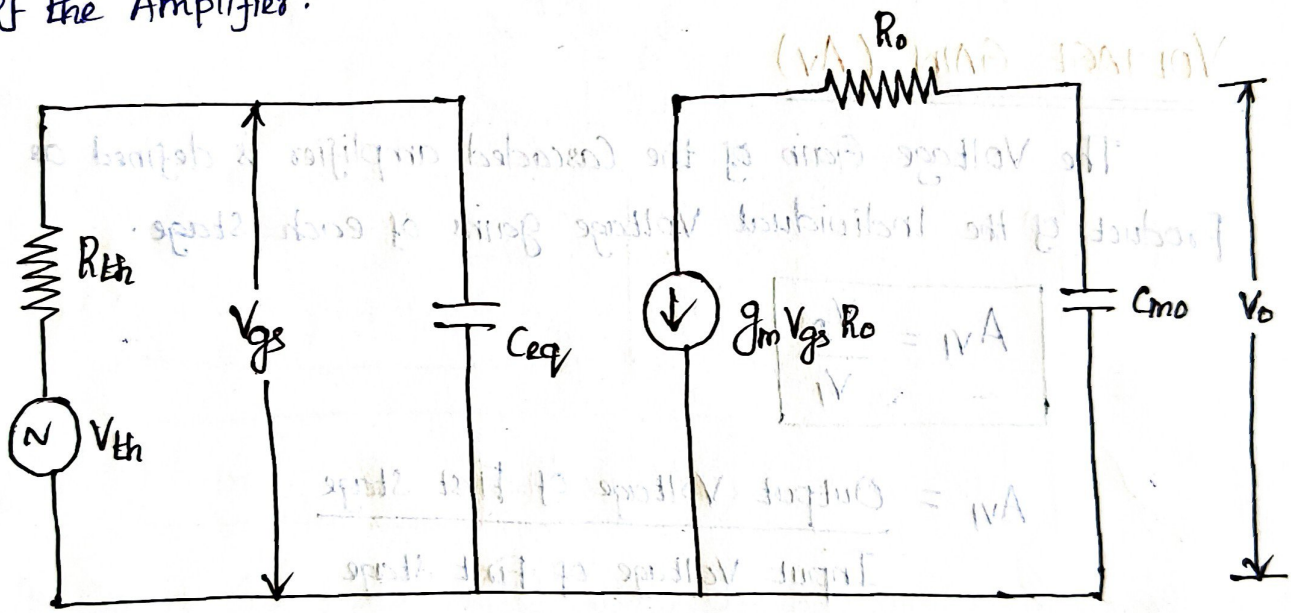


Fig.3. Thevenin's Equivalent Circuit.

FREQUENCY RESPONSE OF MULTI STAGE AMPLIFIERS

NEED OF MULTI-STAGE AMPLIFIERS

1. When Amplification of single stage Amplifier is not sufficient.
2. When Input or Output Impedance is not of correct Magnitude for the Intended Application
3. To Increase the Overall Gain.

Consider the Cascading of 'n' CE Amplifier stages as shown in fig.1.

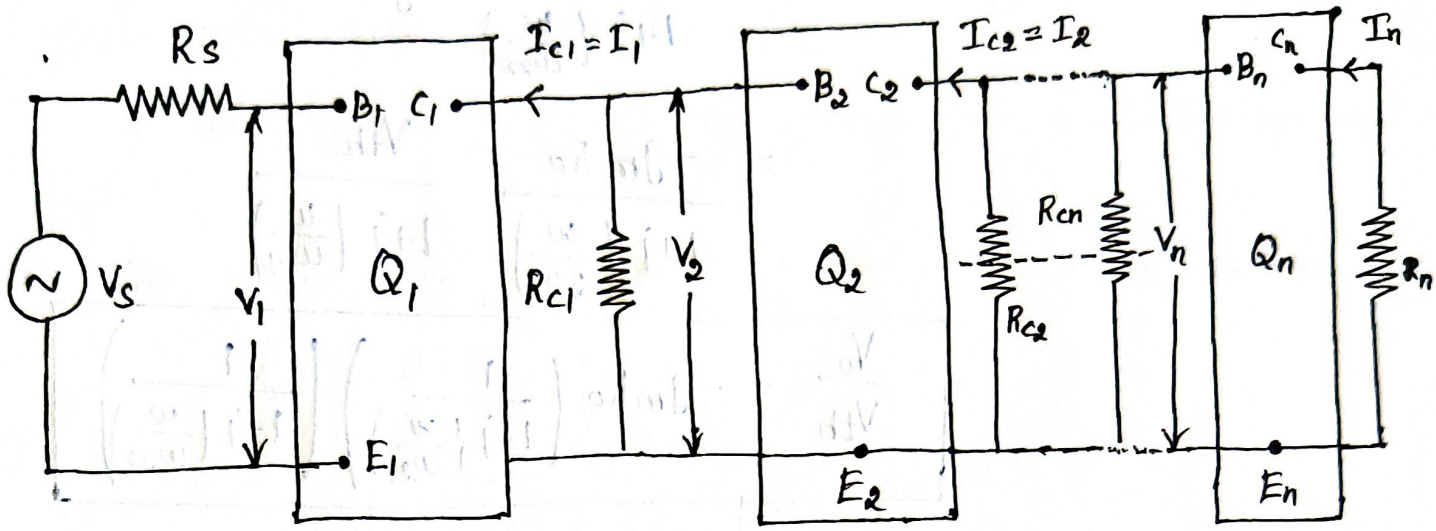


Fig.1. Cascading BJT Amplifier.

VOLTAGE GAIN (A_V)

The Voltage Gain of the Cascaded amplifier is defined as the Product of the Individual Voltage gains of each stage.

$$A_{V1} = \frac{V_2}{V_1}$$

$$A_{V1} = \frac{\text{Output Voltage of First Stage}}{\text{Input Voltage of First Stage}}$$

$$A_{V1} = A_1 \angle \theta_1$$

Where, A_1 - Voltage Gain of the first stage

θ_1 - Phase Angle between Output and Input Voltage of First stage

Total Voltage Gain is written as

$$A_V = \frac{V_o}{V_1} = \frac{V_2}{V_1} \cdot \frac{V_3}{V_2} \cdot \frac{V_4}{V_3} \cdots \frac{V_n}{V_{n-1}} \cdot \frac{V_o}{V_n}$$

$$= A_{V1} \cdot A_{V2} \cdot A_{V3} \cdots A_{Vn-1} \cdot A_{Vn}$$

$$= A_1 \cdot A_2 \cdots A_n \angle \theta_1 + \theta_2 + \cdots \theta_n .$$

$$A_V = A \angle \theta$$

The mag magnitude of Voltage Gain is the product of the magnitudes of the Voltage Gain of Each Stage.

* The phase shift is the sum of phase shift introduced by each stage.

The Voltage Gain can be expressed in terms of Current Gain as

$$A_V = \frac{A_i R_L}{R_i}$$

for n^{th} stage, $\boxed{A_{Vn} = \frac{A_i R_{Ln}}{R_{in}}}$

The Current Gain and Input Impedance of the n^{th} stage is given by,

$$\boxed{A_{in} = \frac{-h_{fe}}{1 + h_{oe} R_{Ln}}}$$

$$\boxed{R_{in} = h_{ie} + h_{re} A_{in} R_{Ln}}$$

The Current Gain and the Input Impedance can be Calculated at every stage by replacing 'n' by the corresponding stage.

UNIT- IV

MULTISTAGE AMPLIFIERS AND DIFFERENTIAL AMPLIFIERS

INTRODUCTION :

If the Voltage and power Gain Obtained from a Single Stage Small signal Amplifier is not Sufficient for a practical Application, More than one Stage of Amplification is used to achieve Necessary Voltage and power Gain. Such an Amplifier is called 'Multistage Amplifier'.

* A Multistage Amplifier using two or more single stage Common Emitter Amplifier (CE) is called as 'Cascaded Amplifiers'.

BISMOS CIRCUITS

The Bipolar Technology uses NPN and PNP Bipolar Junction Transistors (BJT); and the MOS Technology uses NMOS and PMOS Field Effect Transistors (FET)

* The Bipolar Transistors have a Larger Transconductance than MOSFET. MOSFET Circuits have an Infinite Input Impedance, which Indicates a Zero Input Bias Current.

- These advantage of the Two technologies are exploited by Combining Bipolar and MOS Transistors in the Same Integrated Circuit. The technology is called BIMOS or BICMOS. BICMOS technology is useful in digital Circuit design and in Analog Circuits.

BICMOS CASCODE

A Bipolar Cascode Circuit is shown in fig. 1. and corresponding BICMOS configuration is shown in fig. 2.

- The Output Resistance of the Cascode Circuit is Very High. Also the Cascode Amplifier has a wider frequency Bandwidth than the Common-Emitter Circuit, Since the Input Resistance looking into the Emitter of Q_2 is Very Low.

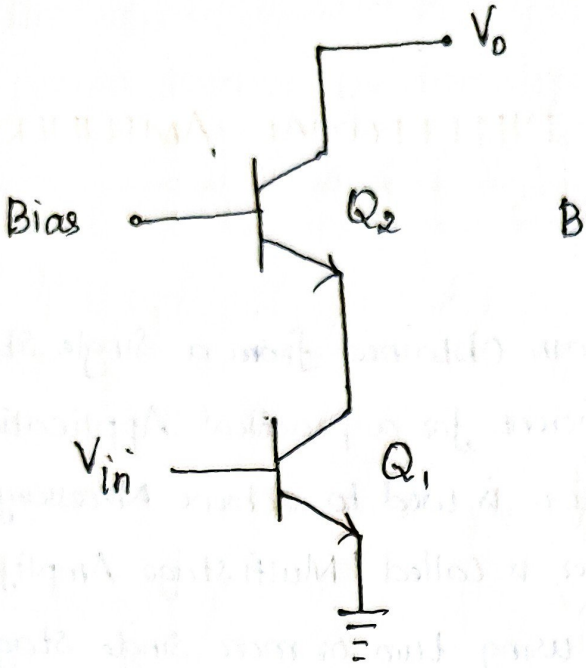


Fig 1. Bipolar Cascode Configuration

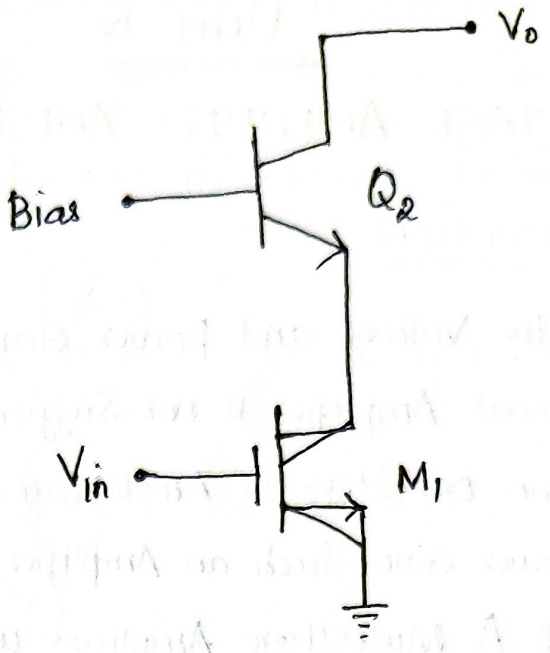


Fig 2. BICMOS Cascode Configuration

The advantage of the BICMOS Circuit is the Infinite Input Resistance of 'M_1'. The Equivalent Resistance Looking into the Emitter (E) of a Bipolar Transistor is much less than the Resistance Looking into the Source (S) of a MOSFET

Therefore the Frequency Response of a BICMOS Cascode Circuit is Superior to that of all MOSFET Cascode Circuit.

BASICS OF DIFFERENTIAL AMPLIFIER

The function of differential Amplifier is to amplify the difference between two Signals. The Need for Differential Amplifies in many Physical Measurements arises where Response from dc to Many Mega-hertz (MHz) is required

- It is also the basic input stage of an Integrated Amplifies.

Fig. 1 shows the basic block diagram of a differential Amplifier in which there are Two Input terminals and one Output terminal. V_1 and V_2 are the two input signals and V_o is the single ended Output.

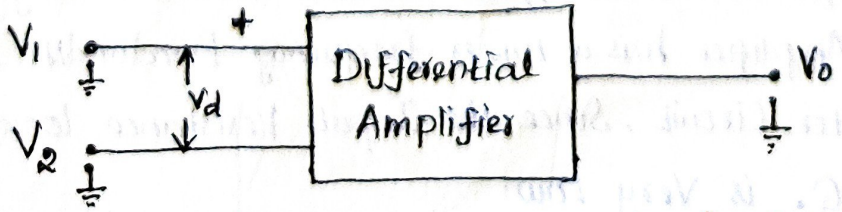


Fig. 1. Block diagram of Differential Amplifier.

The Output Signal in a differential Amplifier is proportional to the difference between the two Input Signals

$$V_o \propto (V_1 - V_2) \quad \text{——} \quad (1)$$

1. DIFFERENTIAL GAIN (A_d)

From the equation (1) we can write,

$$V_o = A_d (V_1 - V_2)$$

Where, A_d - Constant of Proportionality.

A_d is the Gain with which differential Amplifier amplifies the difference between two input signals. Hence it is known as Differential Gain of the differential Amplifier.

$$V_o = A_d V_d$$

Where, V_d - difference Voltage given by $(V_1 - V_2)$

Hence, the differential Gain is given by

$$A_d = \frac{V_o}{V_d}$$

2. COMMON MODE GAIN (A_c)

If two input Voltages which are equal is applied to the differential Amplifier i.e., $V_1 = V_2$, then the Output Voltage $V_o = (V_1 - V_2) A_d$ must be Zero.

* But practically Output Voltage of the differential Amplifier not only depends on the difference Voltage, but also depends on the average of the two inputs. Such an average of the two input signals is called Common Mode Signal denoted as 'V_c'

$$V_c = \frac{V_1 + V_2}{2}$$

Hence, the differential Amplifier also produces the output Voltage proportional to common mode signals

$$V_o = A_c V_c$$

where, A_c - Common Mode Gain

Therefore, there exists some finite Output for $V_1 = V_2$ due to common mode Gain A_c

- Hence the total output of any differential Amplifier can be given as

$$V_o = A_d V_d + A_c V_c$$

3. COMMON MODE REJECTION RATIO (CMRR)

The differential Amplifier is said to be operated in a common mode configuration when the same Voltage is applied to both the inputs i.e, $V_1 = V_2$.

* One of the Requirement of the differential Amplifier is to cancel or reject the Noise Signal that appears as a common Input signal to both the Input terminals of the differential Amplifier.

- The ability of a differential Amplifier to reject a common mode Signal is defined by a ratio called Common Mode Rejection Ratio (CMRR)

* CMRR is defined as the Ratio of the differential Voltage Gain 'Ad' to Common mode Gain 'Ac' and is expressed in dB

$$CMRR = 20 \log \left| \frac{A_d}{A_c} \right| dB$$

In Ideal Cases, Since $A_c = 0$, CMRR $= \infty$

In Practical cases, Since $A_d >> A_c$, CMRR is High

The Output Voltage, can be expressed in terms of CMRR

$$V_o = A_d V_d + A_c V_c$$

$$= A_d V_d \left[1 + \frac{A_c V_c}{A_d V_d} \right]$$

$$V_o = A_d V_d \left[1 + \frac{1}{(A_d/A_c)} \frac{V_c}{V_d} \right]$$

$$V_o = A_d V_d \left[1 + \frac{1}{CMRR} \frac{V_c}{V_d} \right]$$

As CMRR approaches ∞, the output voltage becomes

$$\boxed{V_o = A_d V_d}$$

DIFFERENTIAL AMPLIFIER USING BJT

The transistorised differential Amplifier, basically uses the Emitter biased circuits which are identical in characteristics as shown in figure. 1

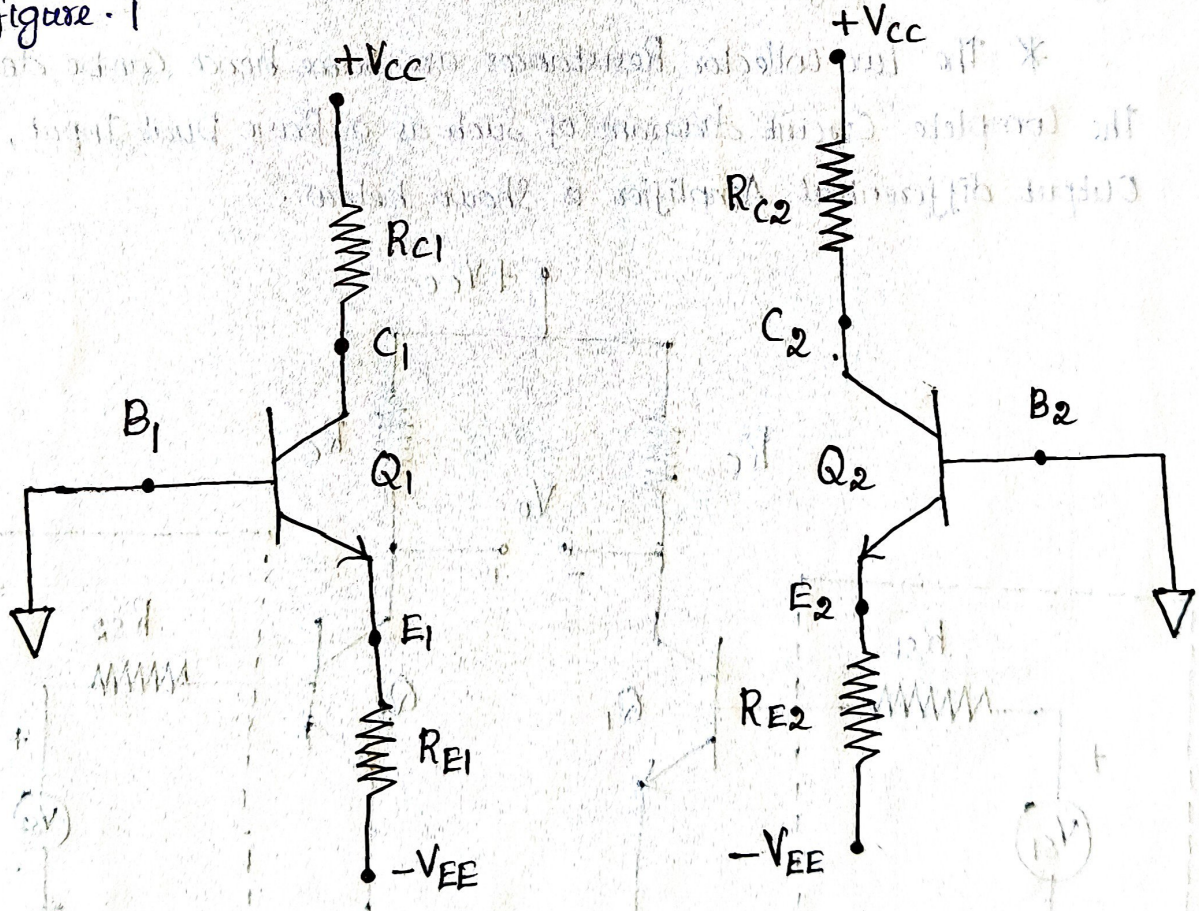


Fig.1. Emitter Biased Circuits

The two transistors Q_1 and Q_2 have exactly matched characteristics. The two collector Resistances R_{C1} and R_{C2} are Equal while the two Emitter Resistances R_{E1} and R_{E2} are also Equal.

Thus $R_{C1} = R_{C2}$ and $R_{E1} = R_{E2}$

the magnitudes of $+V_{CC}$ and $-V_{EE}$ are also same.

- The differential Amplifier can be obtained by using such two Emitter Biased Circuits. This is achieved by connecting Emitter E_1 of 'Q_1' to the Emitter E_2 of 'Q_2'

* Due to this, R_{E1} appears in parallel with R_{E2} and the combination can be replaced by a single Resistance denoted as 'R_E'

- The Base B_1 of 'Q_1' is connected to the Input 1 which is 'V_{S1}' while the Base B_2 of 'Q_2' is connected to the Input 2 which is 'V_{S2}' The Supply voltages are measured with respect to Ground.

• The Balanced Output is taken between the collector C_1 of 'Q_1' and the collector C_2 of 'Q_2'. Such an amplifier is called 'Emitter Coupled differential Amplifier'.

* The two collector Resistances are same hence can be denoted as 'R_C'

The complete Circuit diagram of such as a Basic Dual Input, Balanced Output differential Amplifier is shown below.

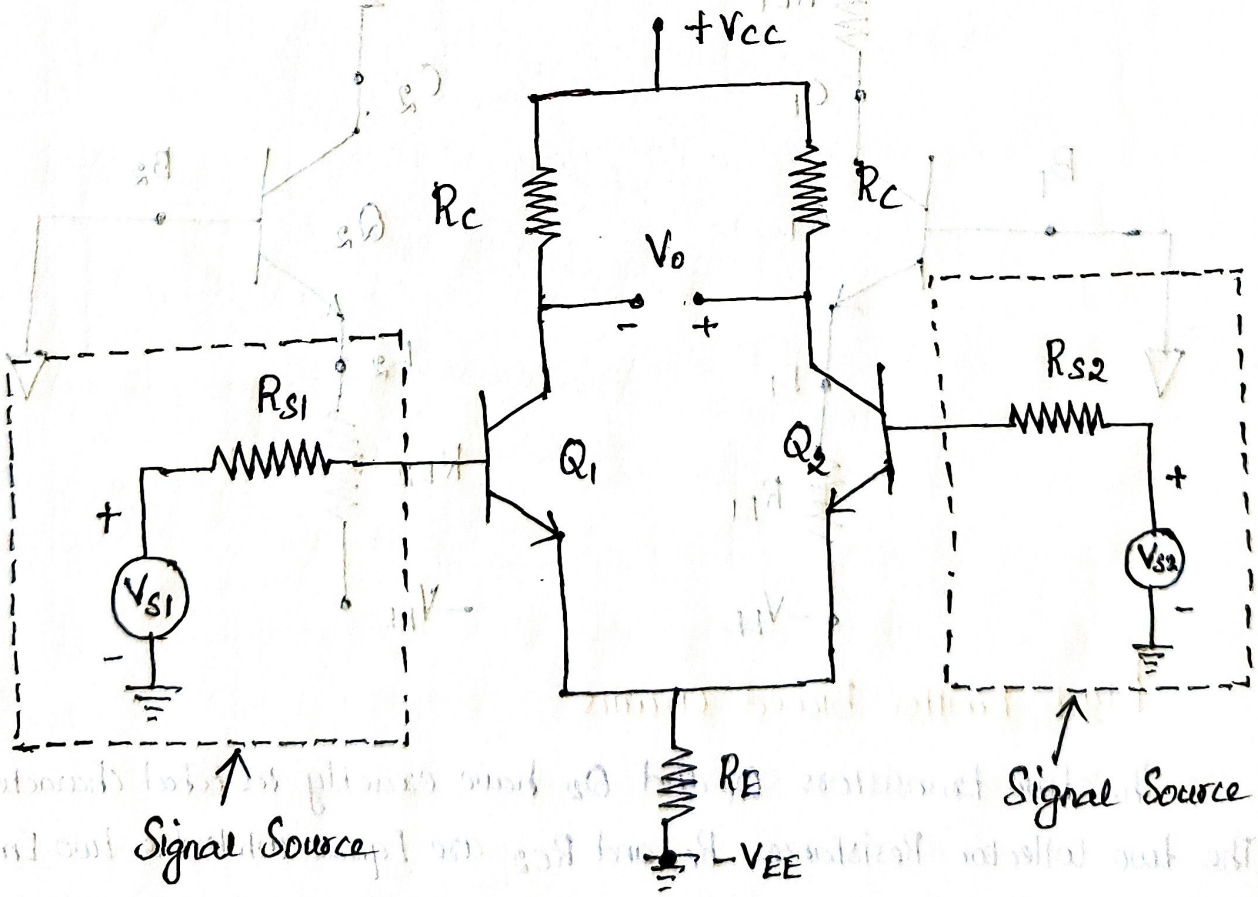


Fig.1. Dual Input, Balanced Output differential Amplifier

As the Output is taken between two output terminals, None of them is grounded, it is called 'Balanced Output Differential Amplifier'

- The Circuit Operation Can be Studied in two modes

i) Differential Mode operation

ii) Common Mode operation.

1. DIFFERENTIAL MODE OPERATION

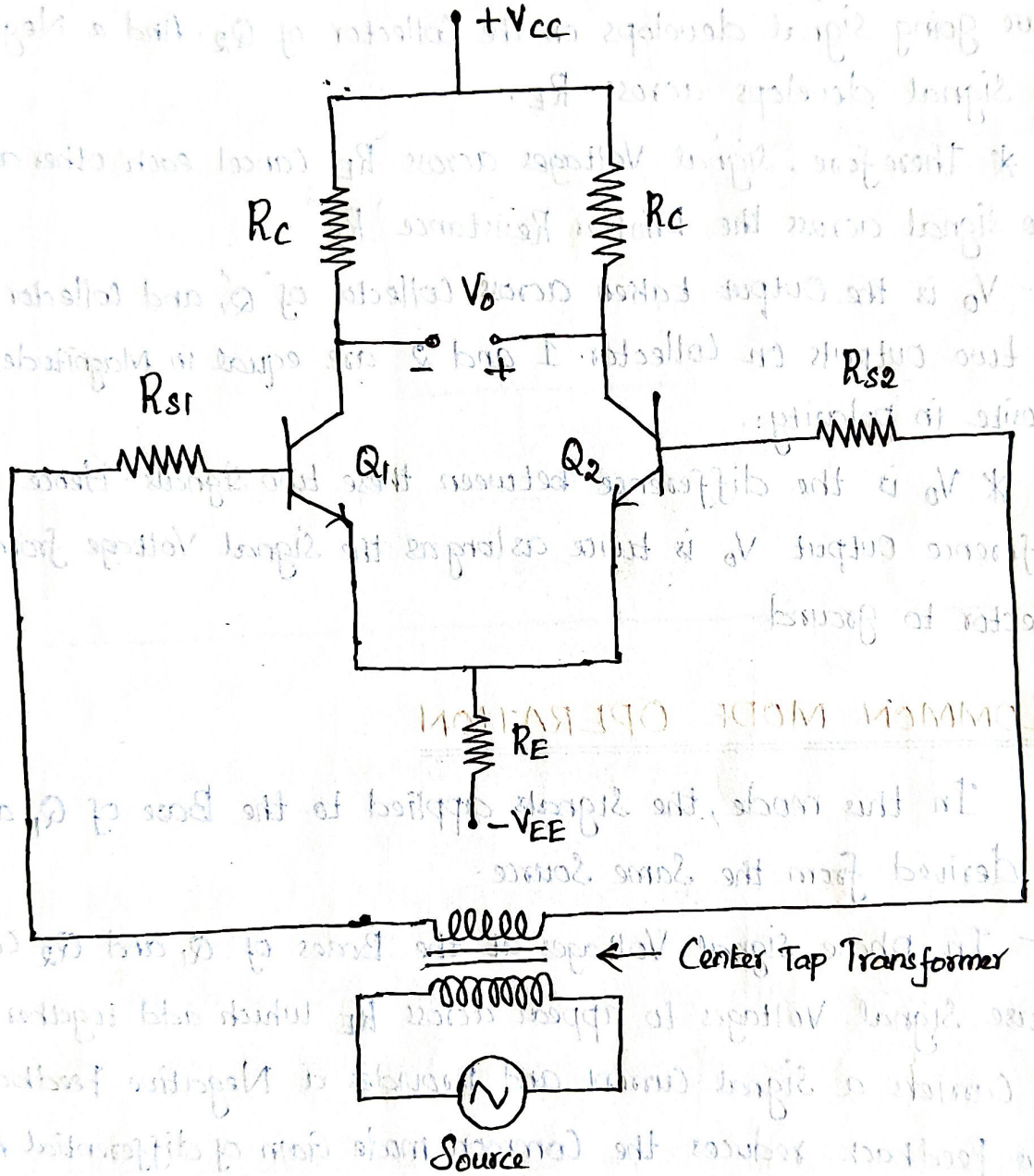


Fig 2: Circuit for differential mode operation.

In the differential mode, the two input signals are different from each other.

* Consider the two input signals which are same in magnitude but 180° out of phase. These signals, with opposite phase can be obtained from the center tap Transformer.

Assume that the Sine wave on the base of Q_1 is positive-going while on the base of Q_2 is Negative-going. With a positive going signal on the Base of Q_1, an amplified Negative going signal develops on the Collector of Q_1.

* Due to positive going signal, Current through R_E also increases and hence a positive going wave is developed across R_E

- Due to Negative going signal on the Base of Q_2 an amplified Positive going signal develops on the Collector of Q_2. And a Negative going signal develops across R_E.

* Therefore, Signal Voltages across R_E Cancel each other and there is No signal across the Emitter Resistance R_E.

- V_o is the Output taken across Collector of Q_1 and Collector of Q_2. The two outputs on Collector 1 and 2 are equal in Magnitude, but opposite in polarity.

* V_o is the difference between these two signals. Hence the difference output V_o is twice as long as the signal Voltage from either Collector to ground

2. COMMON MODE OPERATION

In this mode, the Signals applied to the Base of Q_1 and Q_2 are derived from the Same Source.

- In phase signal Voltages at the Bases of Q_1 and Q_2 causes in Phase Signal Voltages to appear across R_E which add together. Hence R_E Carriers a Signal Current and provides a Negative Feedback. This Feedback reduces the Common mode Gain of differential Amplifier.

* The two signals causes in phase signal Voltages of Equal magnitude to appear across the two collectors of Q_1 and Q_2.

- Now the Output Voltage is the difference between the two Collector Voltages, which are equal and also same in phase (i.e, Zero). Thus the difference Output V_o is almost Zero.

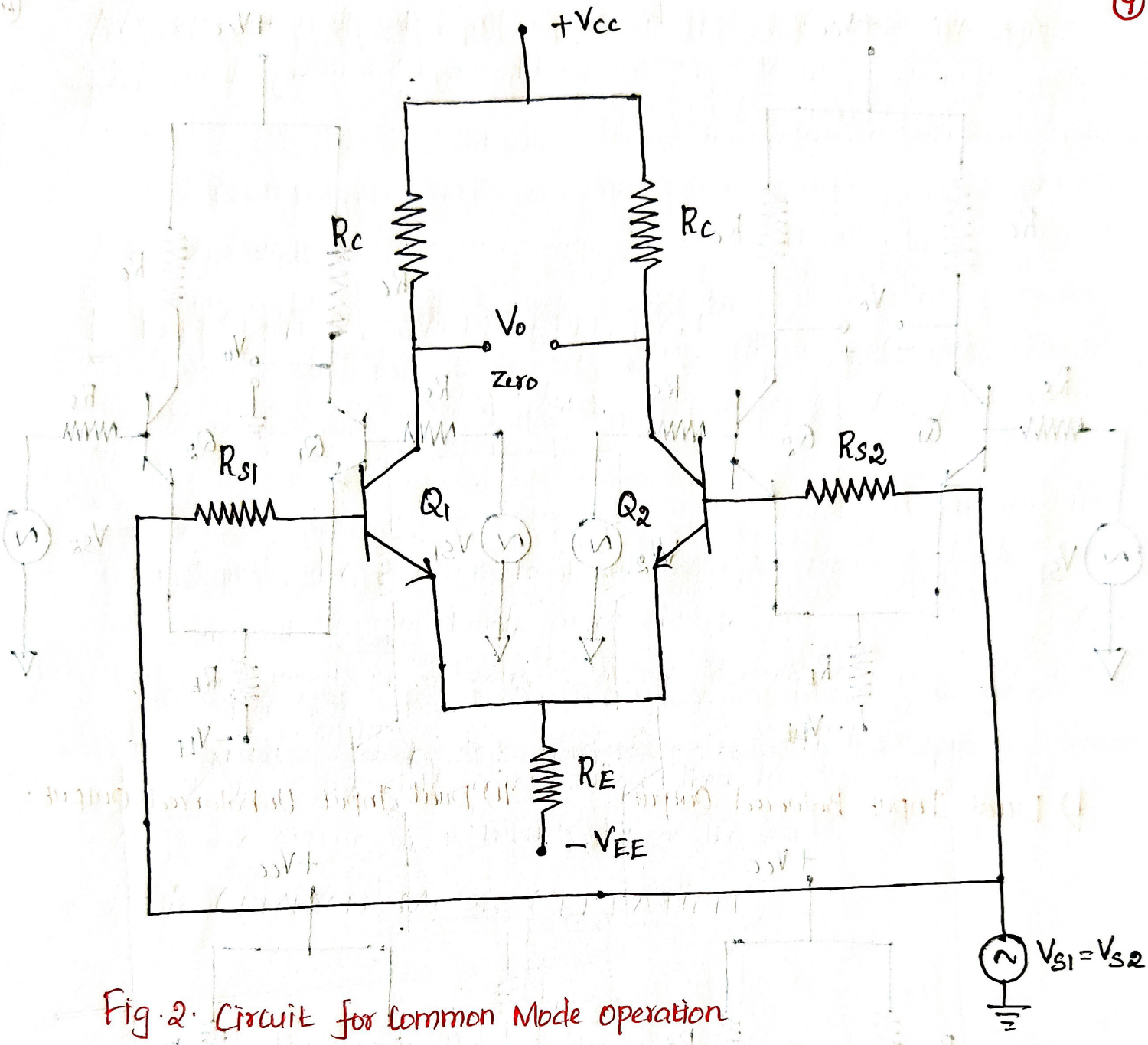


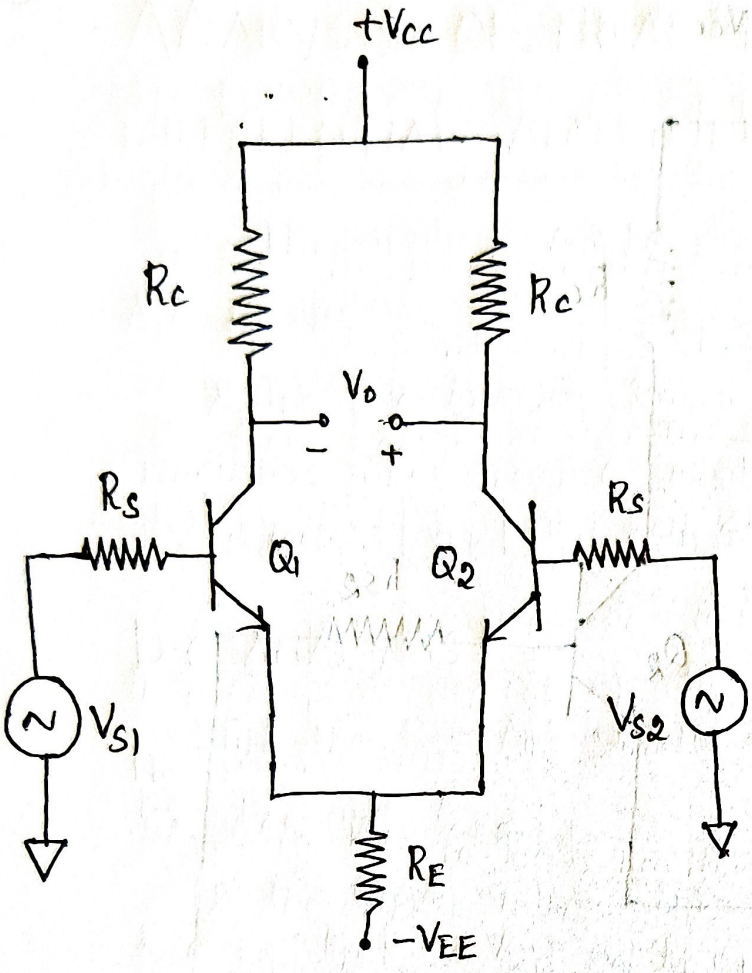
Fig 2. Circuit for common Mode operation

CONFIGURATION OF DIFFERENTIAL AMPLIFIER

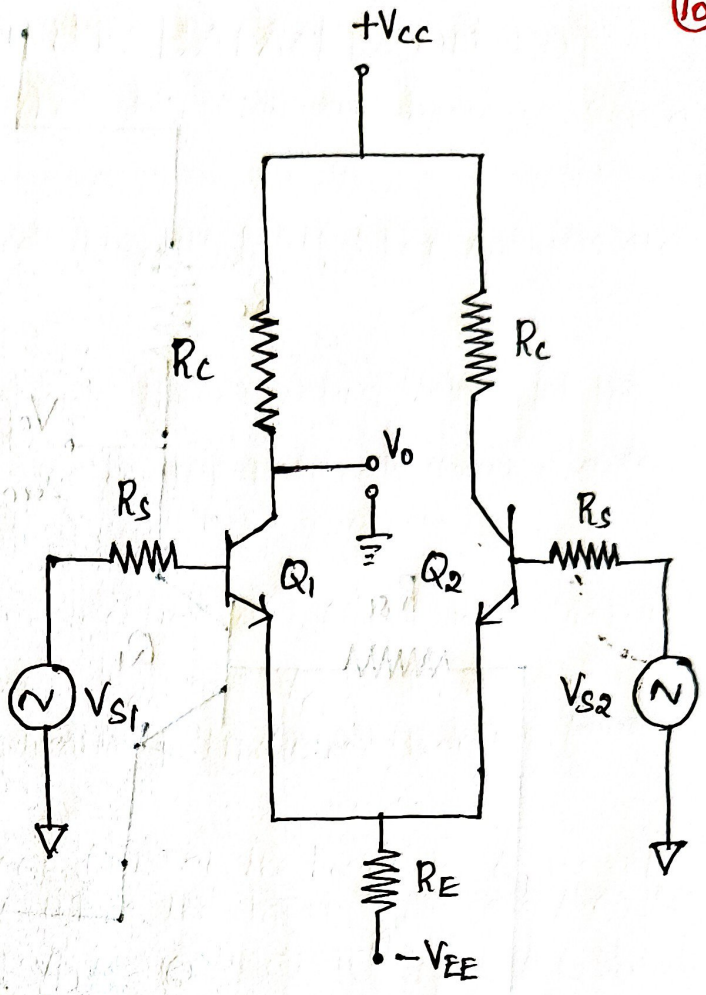
The differential Amplifier in the difference Amplifier stage in the op-amp, can be used in four configurations.

i) Dual Input, Balanced Output differential Amplifier
ii) Dual Input, Unbalanced Output differential Amplifier
iii) Single Input, Balanced Output differential Amplifier.
iv) Single Input, Unbalanced Output differential Amplifier.

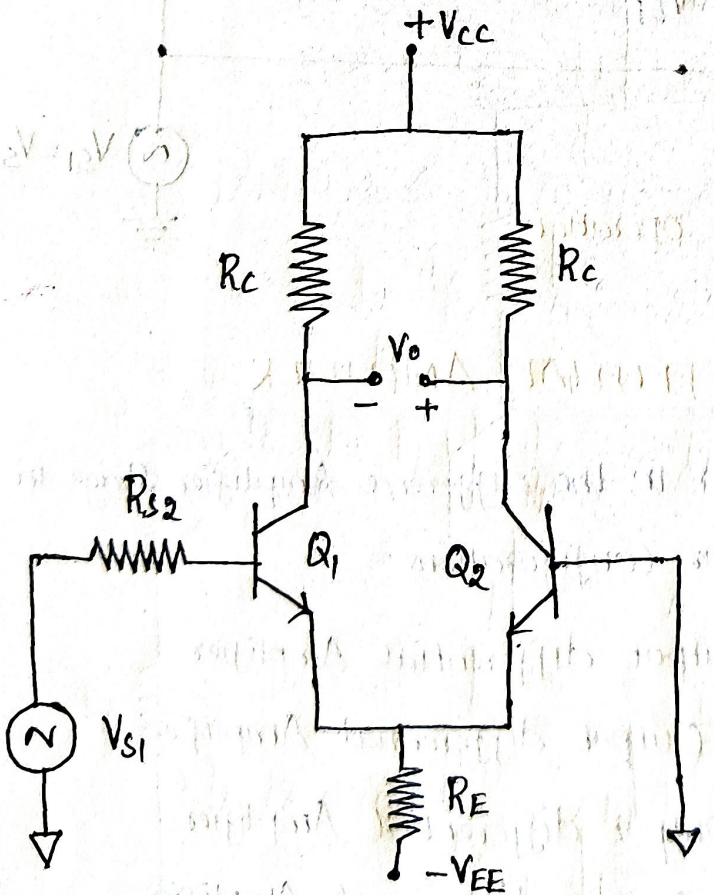
Out of these four configurations, the dual Input, Balanced Output is the basic differential configuration.



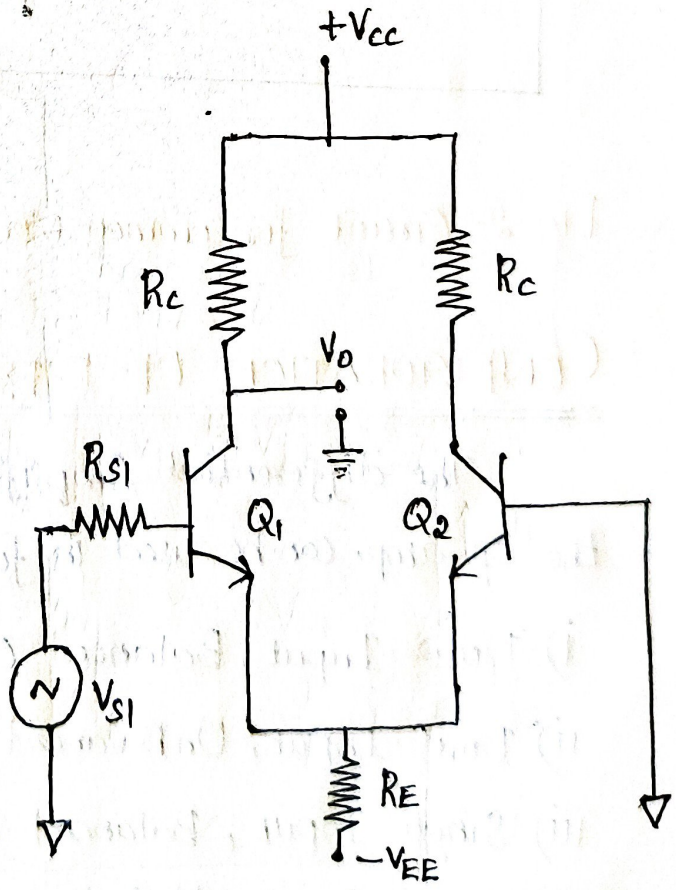
i) Dual Input Balanced Output



ii) Dual Input Unbalanced Output.



iii) Single Input Balanced Output



iv) Single Input Unbalanced Output

Fig. 1. Configuration of Differential Amplifier.

ANALYSIS OF DUAL INPUT, BALACED OUTPUT DIFFERENTIAL AMPLIFIER

The analysis can be divided into two parts : D·C Analysis and A·C Analysis.

* The D·C Analysis Signals decide the operating Values for the Transistors while the A·C signals are the Input signals which decide the Output of the Differential Amplifier.

D·C ANALYSIS

With the D·C Analysis we can attain the operating point Values i.e, I_{CQ} and V_{CEQ}.

* The Supply Voltages are D·C while the Input signals are A·C, so D·C Equivalent Circuit can be obtained by reducing the Input A·C signals to Zero.

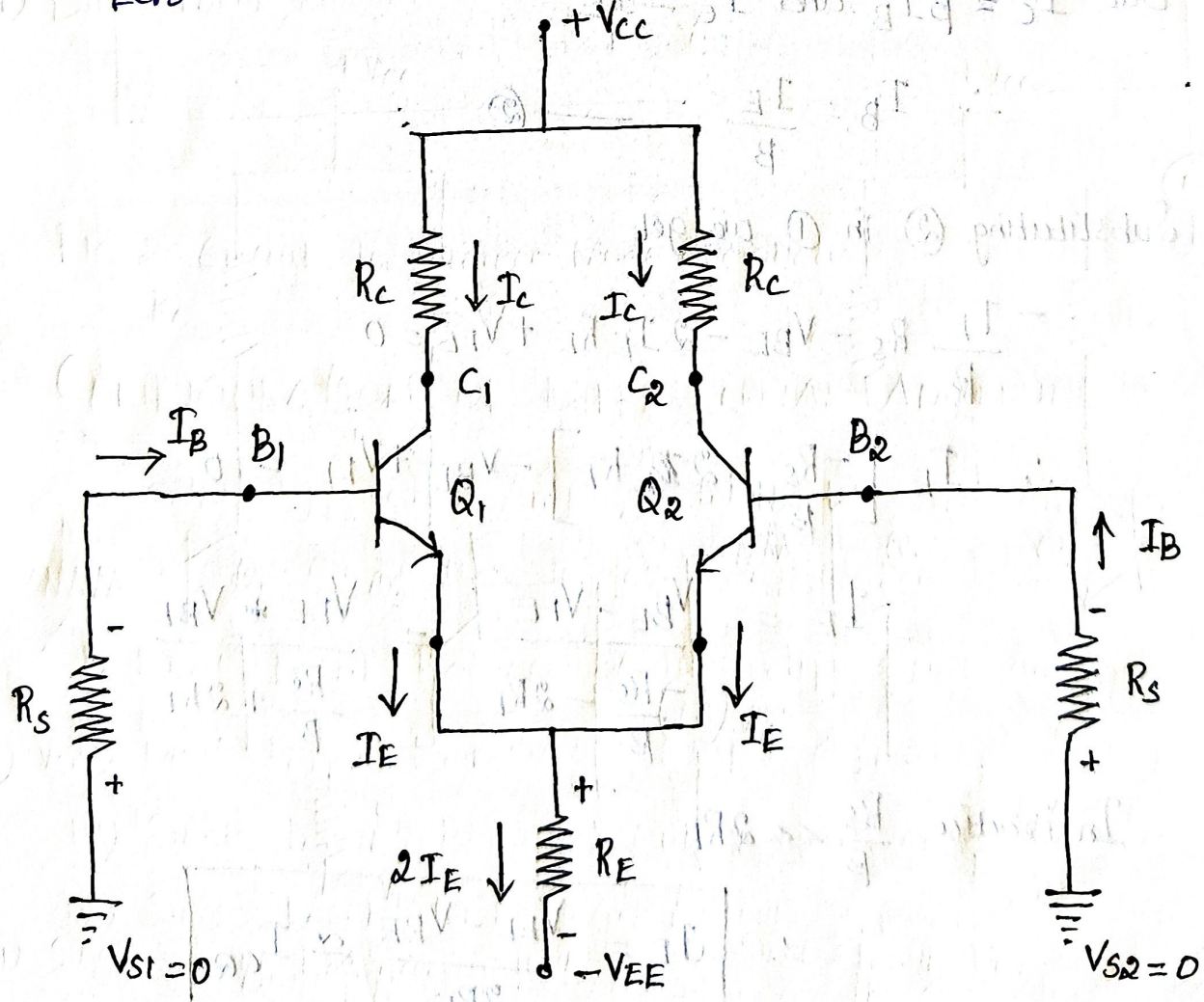


Fig. 1. D·C Analysis

Assuming $R_{S1} = R_{S2}$ the Source Resistance is denoted by 'R_S'

The Transistors Q_1 and Q_2 are matched Transistors and hence for such a matched pair we can assume :

i) Both the Transistors have the same characteristic

ii) $R_{E1} = R_{E2}$ hence $R_E = R_{E1} \parallel R_{E2}$

iii) $R_{C1} = R_{C2}$ hence denoted as R_C

iv) $|V_{CC}| = |V_{EE}|$ and both are measured w.r.t ground.

As the two Transistors are identical and circuit is symmetrical, it is enough to find out operating point I_{CQ} and V_{CEQ} for any one of the two transistors. The same is applicable for the other Transistor

Applying KVL to Base-Emitter Loop (BE) at the transistor Q_1 we get

$$-I_B R_S - V_{BE} - 2 I_E R_E + V_{EE} = 0 \quad \text{——①}$$

But $I_C = \beta I_B$ and $I_C \simeq I_E$

$$\therefore \quad I_B = \frac{I_E}{\beta} \quad \text{——②}$$

Substituting ② in ① we get

$$-\frac{I_E}{\beta} R_S - V_{BE} - 2 I_E R_E + V_{EE} = 0$$

$$\therefore \quad I_E \left[-\frac{R_S}{\beta} - 2 R_E \right] - V_{BE} + V_{EE} = 0$$

$$I_E = \frac{V_{BE} - V_{EE}}{-\frac{R_S}{\beta} - 2R_E} = \frac{V_{EE} + V_{BE}}{\frac{R_S}{\beta} + 2R_E}$$

In Practice $\frac{R_S}{\beta} << 2R_E$

$$\therefore \quad \boxed{I_E = \frac{V_{EE} - V_{BE}}{2R_E} \simeq I_{CQ}}$$

The collector Voltage of Q_1 is

$$V_C = V_{CC} - I_C R_C$$

Neglecting the drop across R_s, the Voltage at the Emitter of Q_1 is approximately equal to $-V_{BE}$.

Hence the collector to Emitter Voltage is

$$V_{CE} = V_C - V_E$$

$$= (V_{CC} - I_C R_C) - (-V_{BE})$$

$$V_{CEQ} = V_{CC} + V_{BE} - I_C R_C$$

2. A.C ANALYSIS

In the A.C analysis the differential Gain Ad, Common mode Gain Ac, Input Resistance Ri and the Output Resistance Ro of the differential Amplifier are calculated using the h-parameters.

i) DIFFERENTIAL GAIN (Ad)

For the differential Gain Calculation, the two Input signals must be different from each other.

- Let the two A.C Input signals be equal in Magnitude but having 180° phase difference between them

* The magnitude of each A.C input Voltage V_{S1} and V_{S2} be $\frac{V_s}{2}$

The two A.C Emitter Currents I_{E1} and I_{E2} are equal in magnitude and 180° out of phase. Hence they Cancel each other to get resultant A.C Current through the Emitter is Zero.

The approximate Hybrid Model for the above circuit can be Shown as below in fig. 2.

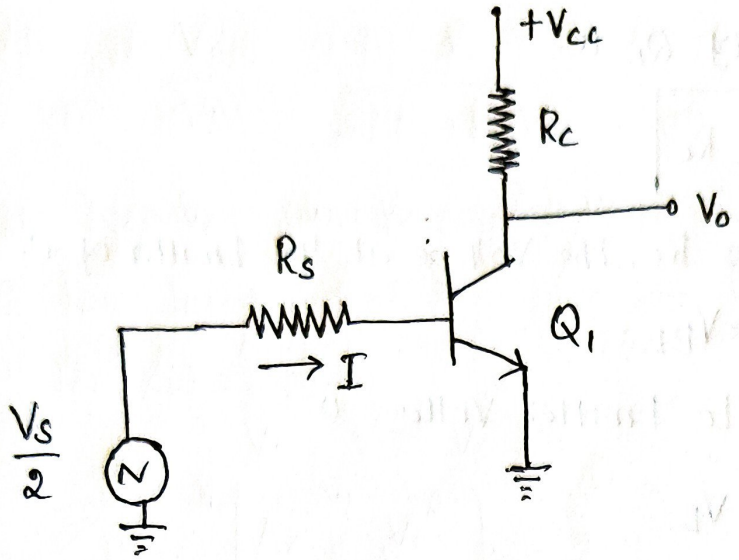


Fig.1. A.C Equivalent for Differential operation.

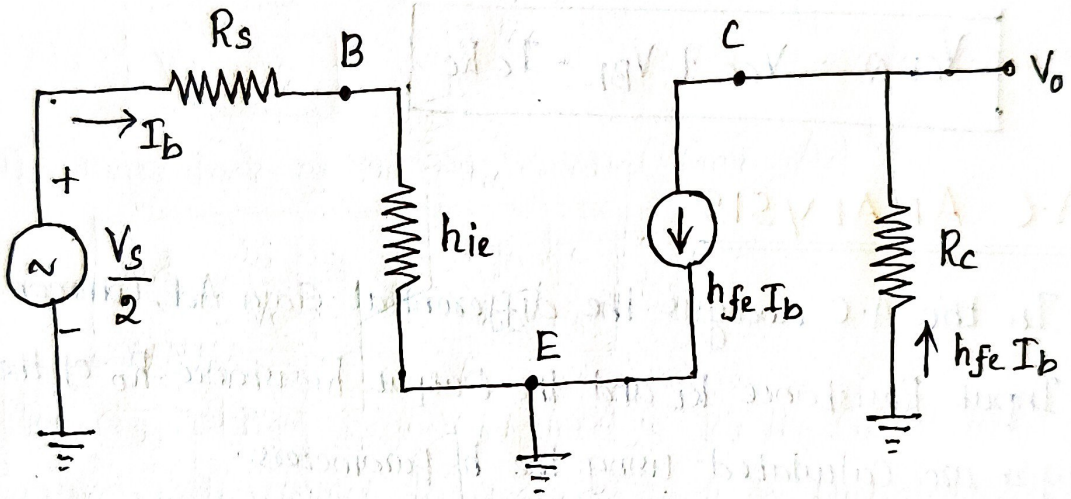


Fig.2. Approximate Hybrid Model.

Applying KVL to the Input Loop

$$-I_b R_s - I_b h_{ie} + \frac{V_s}{2} = 0 \quad \text{——①}$$

$$-I_b (R_s + h_{ie}) = -\frac{V_s}{2}$$

$$\boxed{I_b = \frac{V_s}{2(R_s + h_{ie})}} \quad \text{——②}$$

Applying KVL to the Output Loop

$$V_o = -h_{fe} I_b R_c \quad \text{——③}$$

Substituting ② in ③

$$V_o = -h_{fe} I_b \left(\frac{V_s}{2(R_s + h_{ie})} \right)$$

$$\frac{V_o}{V_s} = \frac{-h_{fe} R_c}{2(R_s + h_{ie})}$$

The Negative sign indicates the phase difference between Input and Output The two Input Signal magnitudes are $\frac{V_s}{2}$ but they are opposite in polarity, as 180° out of phase

$$\therefore V_d = V_1 - V_2$$

$$= \frac{V_s}{2} - \left(\frac{-V_s}{2}\right)$$

$$\boxed{V_d = V_s}$$

The magnitude of the differential Gain Ad is

$$\boxed{A_d = \frac{V_o}{V_s} = \frac{1}{2} \frac{h_{fe} R_c}{R_s + h_{ie}}}$$

The differential gain obtained is for the circuit where output is measured with aspect to ground. So it is 'Unbalanced Output'

* Balanced Output is across the two collectors of the transistors Q_1 and Q_2. Such Balanced Output is double than that obtained above with unbalanced output.

– Hence the Expression for Ad with Balanced Output changes as

$$A_d = 2 \times \frac{h_{fe} R_c}{2(R_s + h_{ie})}$$

$$\boxed{A_d = \frac{h_{fe} R_c}{R_s + h_{ie}}} \text{ (Magnitude).}$$

This is the differential Gain for balanced Output Dual Input differential Amplifier circuit.

ii) COMMON MODE GAIN (A_c)

Let the magnitude of both the A.C input signals be 'Vs' and are in phase with each other.

Hence the differential input $V_d = 0$ while the common mode Input V_c is the average value of the two.

$$V_C = \frac{V_1 + V_2}{2} = \frac{V_s + V_s}{2} = \frac{2V_s}{2} = V_s.$$

While the Output can be expressed as

$$V_o = A_c \cdot V_s$$

$$\boxed{A_c = \frac{V_o}{V_s}}$$

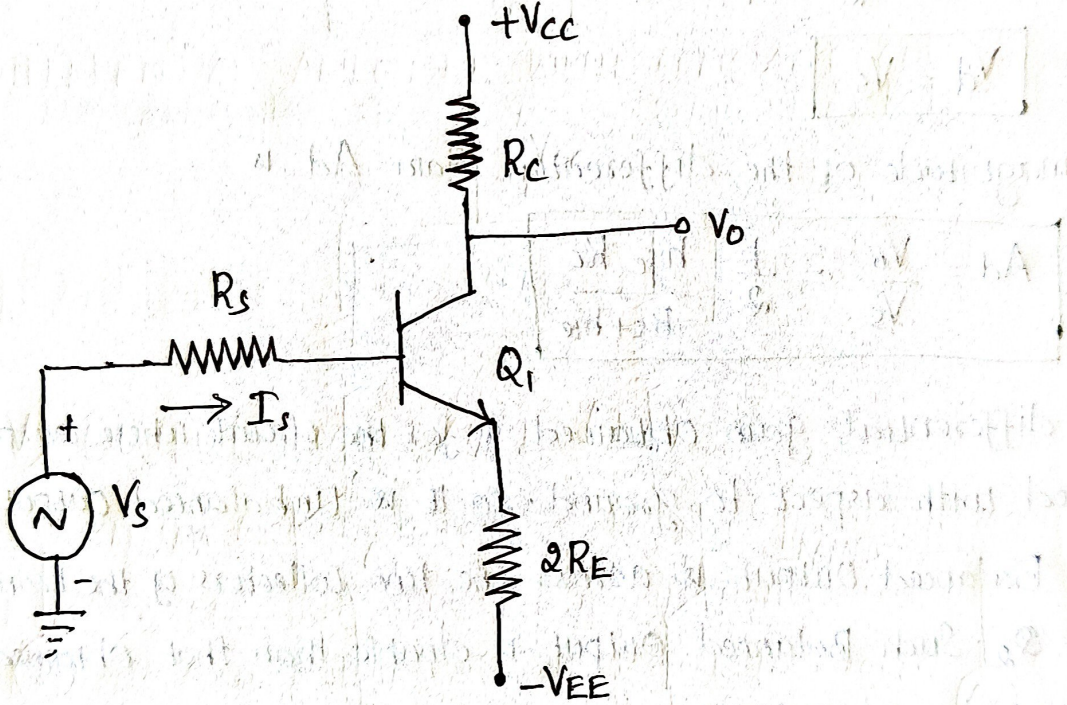


Fig. 3. A.C Equivalent for common mode operation.

iii) COMMON MODE REJECTION RATIO (CMRR)

$$CMRR = 20 \log_{10} \left| \frac{A_d}{A_c} \right|$$

Substituting the results of Ad and Ac, we get.

$$CMRR = 20 \log_{10} \left| \frac{h_{fe} R_c}{(R_s + h_{ie})} \cdot \frac{R_s + h_{ie} + 2R_E(1 + h_{fe})}{h_{fe} R_c} \right|$$

$$CMRR = 20 \log_{10} \left| \frac{R_s + h_{ie} + 2R_E(1 + h_{fe})}{R_s + h_{ie}} \right| \text{ dB for Balance Output}$$

$$CMRR = 20 \log_{10} \left| \frac{R_s + h_{ie} + 2R_E(1+h_{fe})}{2(R_s + h_{ie})} \right| \text{ dB for Unbalanced Output.}$$

iv) INPUT IMPEDANCE (R_i)

The Input Impedance R_i can be defined as the equivalent Resistance existing between any one of the inputs and the ground when the other input is grounded.

Therefore, $\boxed{R_i = \frac{V_s}{I_b}}$ $\qquad I_b = \frac{V_s}{2(R_s + h_{ie})}$

We can write $R_i = \frac{V_s}{I_b} = \frac{2(R_s + h_{ie}) I_b}{I_b}$

$$\boxed{R_i = 2(R_s + h_{ie})}$$

V) OUTPUT IMPEDANCE (R_o)

The Output Impedance R_o is defined as the equivalent Resistance between one of the Output terminals with respect to Ground. The Resistance between Output terminal with respect to Ground is R_c

$$\therefore \boxed{R_o = R_c}$$

METHODS OF IMPROVING CMRR

Higher the Value of CMRR, better is the performance of differential Amplifier. Hence in practice the efforts are always to improve the CMRR of the differential Amplifier.

EFFECT OF R_E

To improve the CMRR, the Common mode Gain 'A_c' must be reduced. The Common mode Gain A_c approaches Zero as R_E tends to Infinity.

- This is because R_E introduces a Negative Feedback in the Common Mode operation which reduces the Common Mode Gain 'A_c'

Thus higher the Value of R_E, lesser is the Value of Ac and higher is the Value of CMRR. The differential Gain 'Ad' is not dependent on 'R_E'

* But practically R_E cannot be Selected Very high because Large R_E needs higher biasing Voltage to the Set the Operating Q point of the Transistor.

- Hence, Practically instead of increasing R_E Various Other methods are used which provide effect of increased R_E without any Limitations.

i) Constant Current Circuit Method
ii) Use of Current Mirror Circuit.

DIFFERENTIAL AMPLIFIER WITH CONSTANT CURRENT CIRCUIT

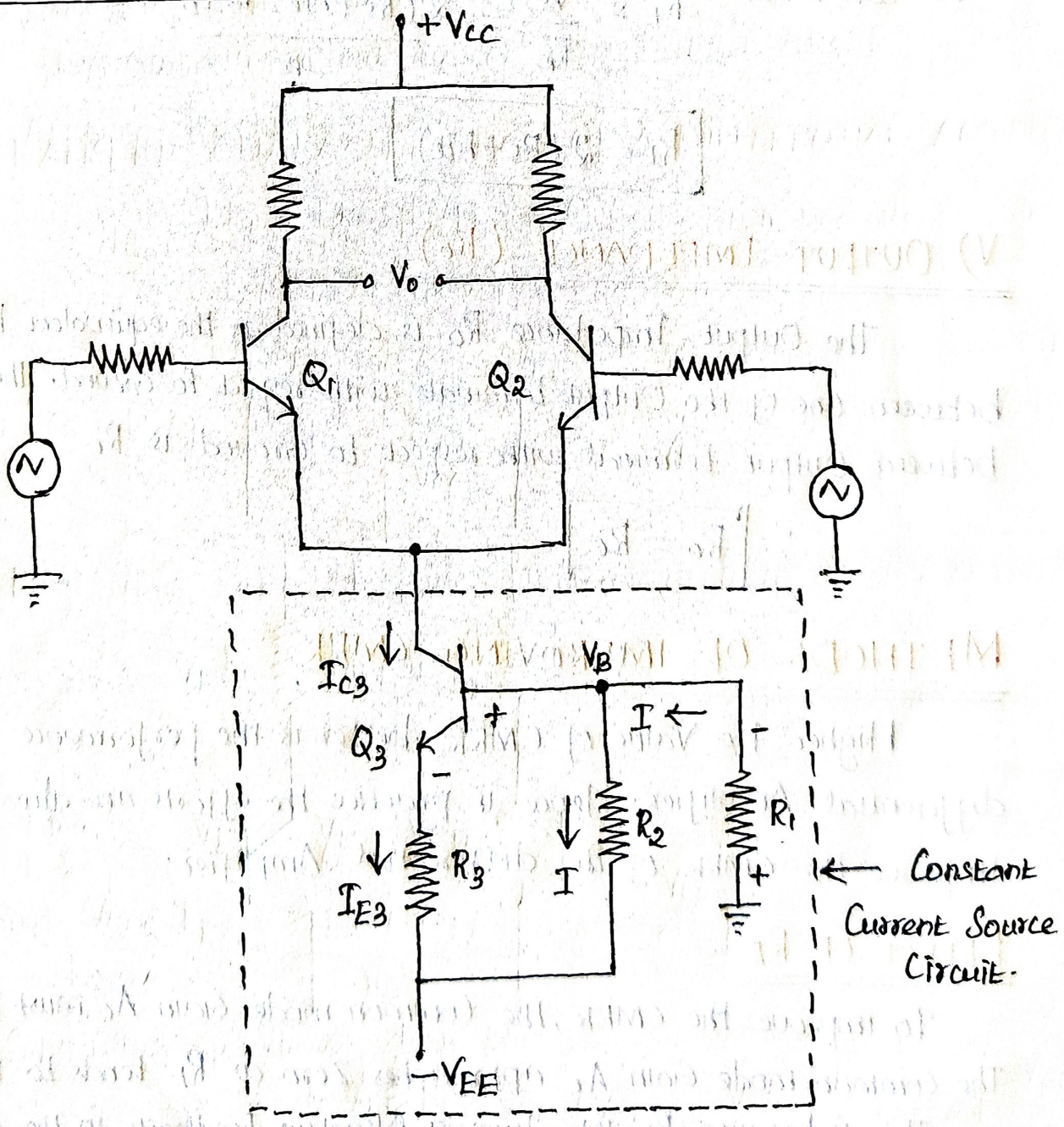


Fig.1. Differential Amplifier with Constant Current Circuit.

Without physically increasing the value of R_E, the R_E is replaced by a Transistor operated at a constant current. Such a constant current source circuit gives the Effect of a very high Resistance without affecting the 'Q point' values of the Differential Amplifier.

* The transistor used is Q_1 and the values of R_1, R_2 and R_3 are selected so as to give the same operating point values for the two transistors Q_1 and Q_2.

CIRCUIT ANALYSIS

Let current flow through R_3 be I_3, while current through R_1 is I Neglecting the Base current of Q_3 which is very small due to Large β_{ac}. - we can assume that current through R_2 is also I

Applying Kirchhoff's Law,

$$-IR_1 - IR_2 + V_{EE} = 0$$

$$-I(R_1+R_2) + V_{EE} = 0$$

$$-I(R_1+R_2) = -V_{EE}$$

$$\boxed{I = \frac{V_{EE}}{R_1+R_2}} \quad \text{——} (1)$$

Now $V_B = -IR_1$, Negative sign according to the direction of current

$$\therefore V_B = \frac{-V_{EE} R_1}{R_1+R_2} \quad \text{——} (2)$$

Now $$V_E = V_B - V_{BE} \quad \text{——} (3)$$

and $$I_{E3} = \frac{V_E - (-V_{EE})}{R_3} \quad \text{——} (4)$$

Substituting eqns (1), (2), (3) in (4)

$$I_{E3} = \frac{\frac{-V_{EE} R_1}{R_1+R_2} - V_{BE} + V_{EE}}{R_3} = \frac{V_{EE}\left[1 - \frac{R_1}{R_1+R_2}\right] - V_{BE}}{R_3}$$

$$I_{E3} = \frac{V_{EE}\left[\frac{R_1+R_2-R_1}{R_1+R_2}\right] - V_{BE}}{R_3} = \frac{V_{EE}\left[\frac{R_2}{R_1+R_2}\right] - V_{BE}}{R_3}$$

Neglecting I_{B3} we can write

$$I_{E3} = I_{B3}.$$

Thus as V_{EE}, R_1, R_2, R_3 and V_{BE} are constants, Current I_{C3} is almost equal to I_{E3} ($I_{E3} \simeq I_{C3}$) and also constant. Thus Circuit with transistor Q_3 acts as a Constant Current Source.

* Practically there is substantial increase in CMRR due to constant Current Bias without increasing biasing voltages and without disturbing Q point values of Q_1 and Q_2.

TRANSFER CHARACTERISTICS OF A DIFFERENTIAL AMPLIFIER

The dc transfer characteristic is useful in understanding the Large signal behaviour of the differential Amplifier.

– This is important because the transfer characteristics shows that the circuit operation is Linear over a Limited Range of Input Voltage.

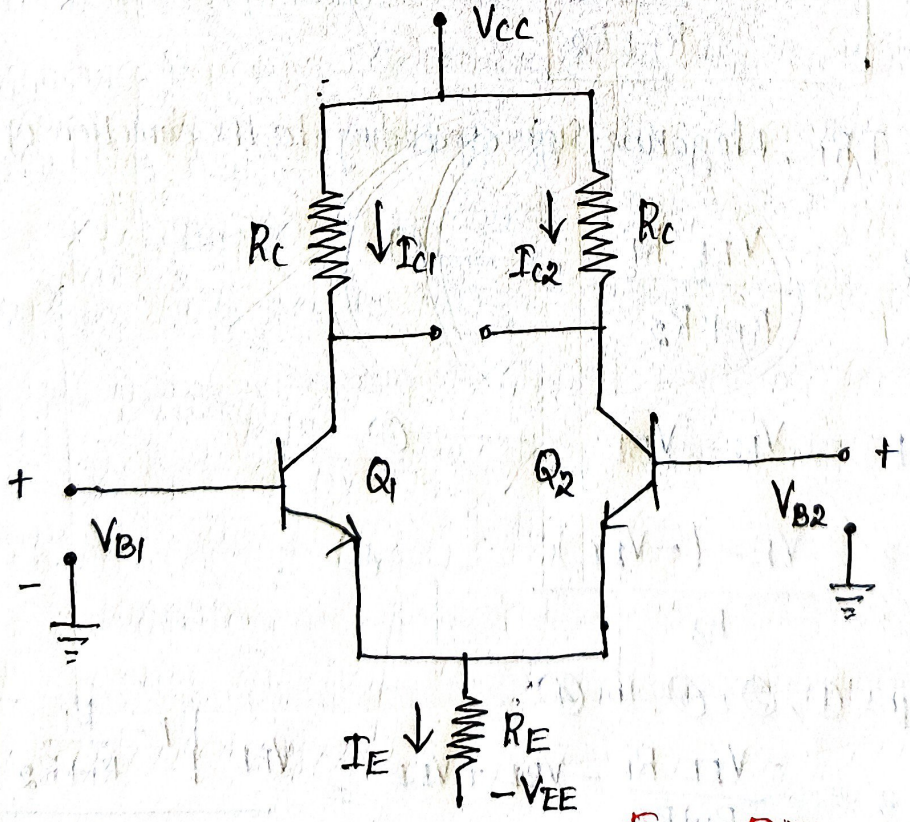


Fig.1 Differential Amplifier.

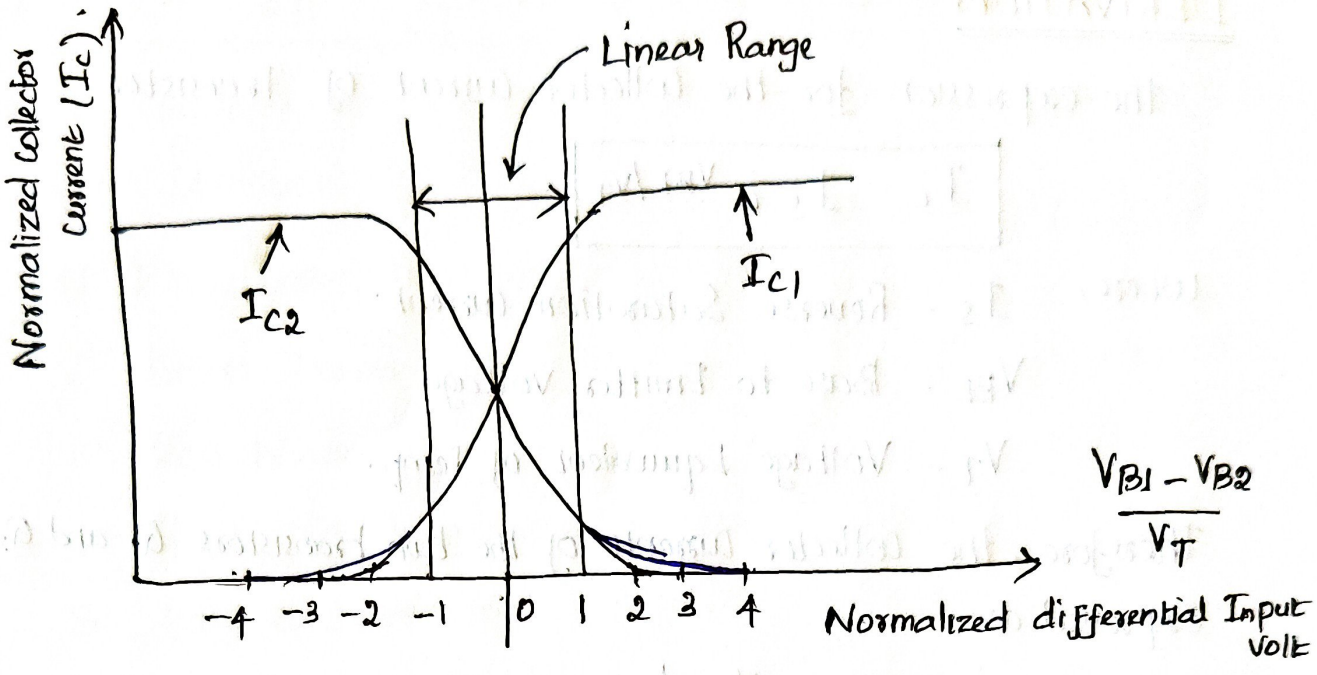


Fig. 2. Normalized differential Input Volt.

In the transfer characteristics of a differential Amplifier, the graph is between Normalized differential Input Voltage Versus the Normalized Collector Current.

- The Normalized differential Input Voltage is defined as the Ratio of $\frac{V_d}{V_T}$

* For the Negative Values of Normalized differential Input Voltage, $(V_{B1} - V_{B2})$ is Negative. That means V_{B1} is Smaller than V_{B2}. Therefore Transistor Q_2 will Conduct more than Transistor Q_1.

- For Normal differential Input Volt higher than $-4V$, Q_1 is OFF and Q_2 only is ON. Therefore only I_{C2} will flow. For the differential Input between $-4V$ and $0V$, both transistor Conduct with $I_{C2} > I_{C1}$.

* And at 0V differential Input Voltage, both the transistors Conduct equally (i.e.,) $I_{C1} = I_{C2}$

- With increase in the Normalized differential Input Voltage in the positive direction, Q_1 starts Conducting more and Q_2 goes towards Cut off.

DERIVATION

The expression for the Collector Current of Transistor

$$I_C = I_S e^{V_{BE}/V_T}$$

where, I_S - Reverse Saturation Current.

V_{BE} - Base to Emitter Voltage

V_T - Voltage Equivalent of Temp.

Therefore, the collector currents of the two transistors Q_1 and Q_2 can be expressed as

$$I_{C1} = I_S e^{V_{BE1}/V_T}$$

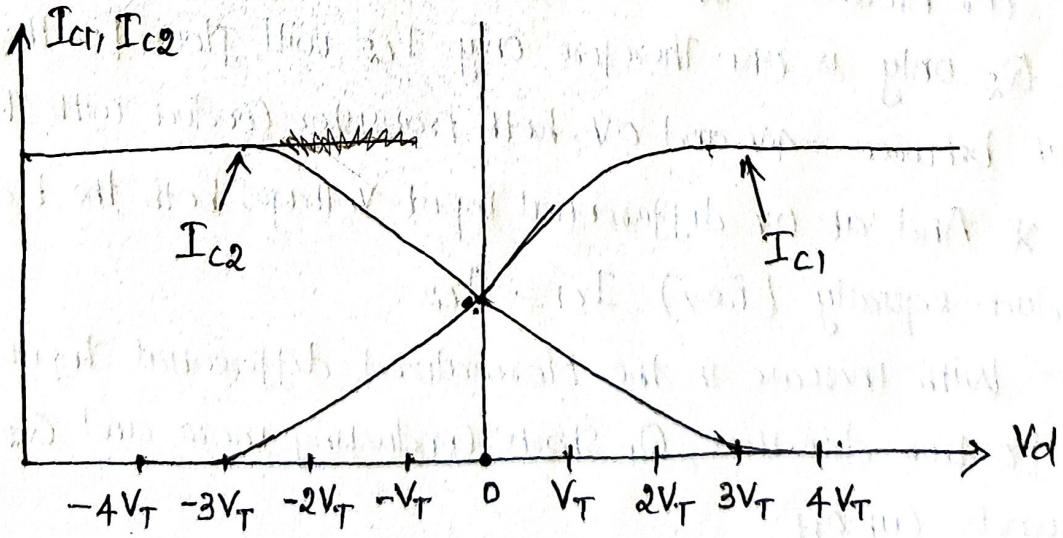
$$I_{C2} = I_S e^{V_{BE2}/V_T} \quad (I_{S1} = I_{S2} = I_S)$$

Taking the Natural Log on both the sides we get

$$\ln \frac{I_{C1}}{I_S} = \frac{V_{BE1}}{V_T}$$

$$V_{BE1} = V_T \ln \left[\frac{I_{C1}}{I_S}\right]$$

and $$V_{BE2} = V_T \ln \left[\frac{I_{C2}}{I_S}\right]$$



FET DIFFERENTIAL AMPLIFIER

A differential Amplifier using JFET or MOSFET offers the following advantages compared to BJT.

1. High Input Impedance
2. Better Thermal Stability
3. Less Noise
4. Drift with Temperature is Less
5. Easy to Fabricate
6. Complexity is Reduced
7. Very Low Bias and OFFset Currents.

The only factor that limits the performance of JFET and MOSFET compared to BJT is their Low gain-bandwidth (GBW) product.

* Similar to differential BJT Amplifier, FET differential Amplifier Can be broadly classified into the following four configurations.

i) Single Input, Balanced Output Differential Amplifier.
ii) Single Input, Unbalanced Output Differential Amplifier.
iii) Dual Input, Balanced Output differential Amplifier.
iv) Dual Input, Unbalanced Output Differential Amplifier.

Let us Analyse and determine the CMRR of a dual input Unbalanced Output differential Amplifier using JFET.

DUAL INPUT UNBALANCED OUTPUT FET DIFFERENTIAL AMPLIFIER

The Circuit of dual input Unbalanced Output differential Amplifier using JFET is shown in fig. 1.

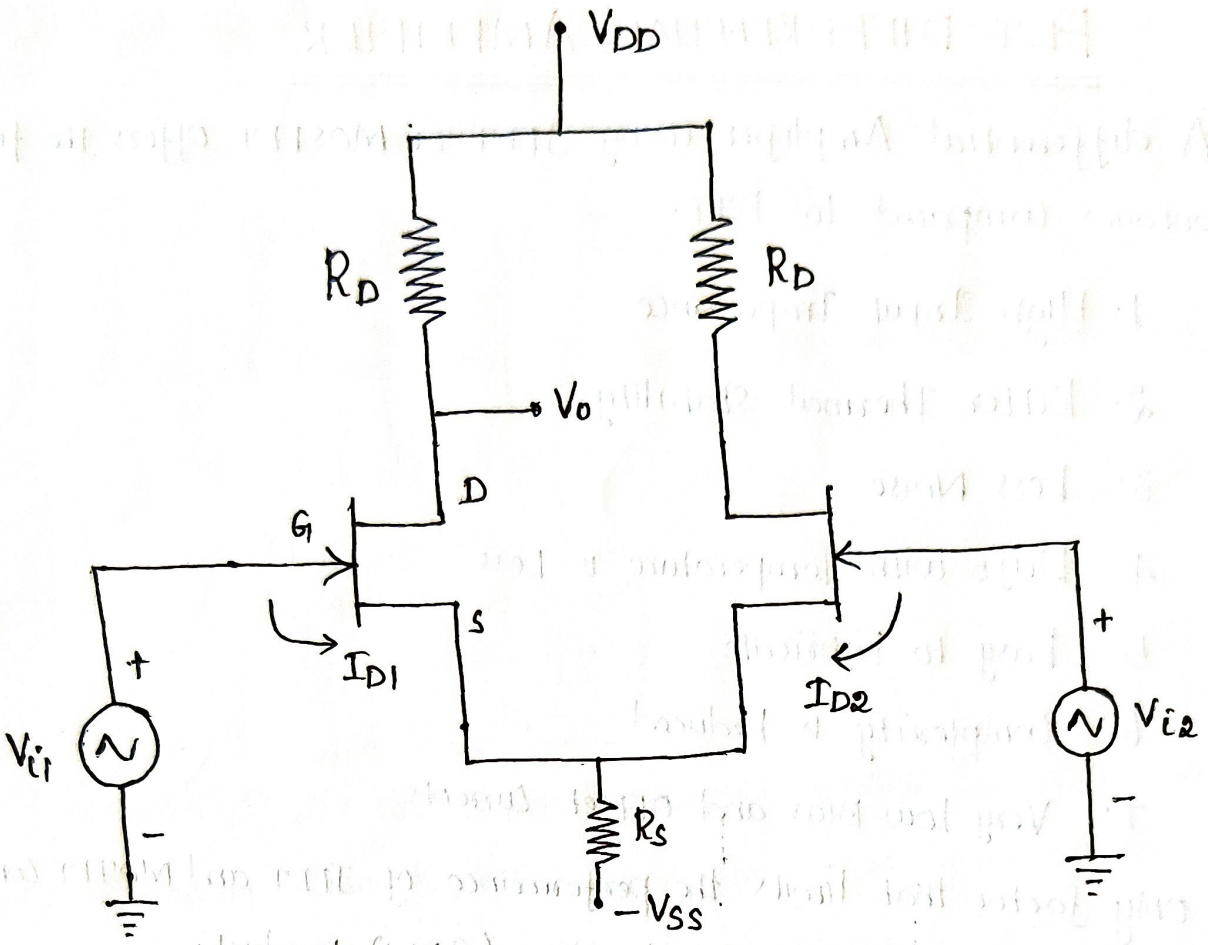


Fig.1 Dual Input Unbalanced Output JFET differential Amplifier.

1. DC ANALYSIS

For dc Analysis, the Effect of a A.C is removed by Short-circuiting the Sources. Hence, the Circuit is reduced as shown in fig. 2.

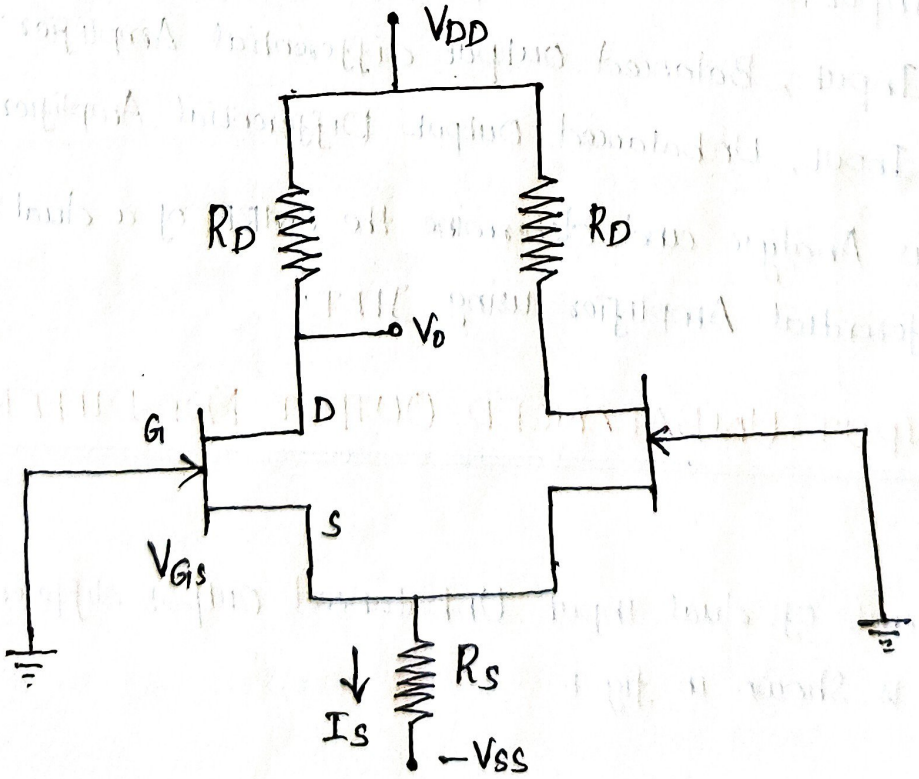


Fig.2. DC Equivalent

From the Circuit, $\boxed{I_S = I_{D1} + I_{D2}}$

If the devices are assumed to be identical then

$$I_S = 2 I_D \quad \text{or} \quad I_D = \frac{I_S}{2} \qquad \text{——} (1)$$

To determine Source Current I_S, apply KVL to the Input loop

$$V_{GS} + I_S R_S - V_{SS} = 0$$

$$I_S R_S = V_{SS} - V_{GS}$$

$$\boxed{I_S = \frac{V_{SS} - V_{GS}}{R_S}} \qquad \text{——} (2)$$

From eqn (2), we can determine Source Current I_S. Once Source Current I_S is known, drain current I_D is calculated from eqn (1)

Applying KVL to the Output Loop of the device, we get

$$V_{DD} - I_D R_D - V_{DS} - I_S R_S + V_{EE} = 0$$

$$\boxed{V_{DS} = V_{DD} + V_{EE} - I_D R_D - I_S R_S}$$

Thus the operating Parameters are found

2. AC ANALYSIS

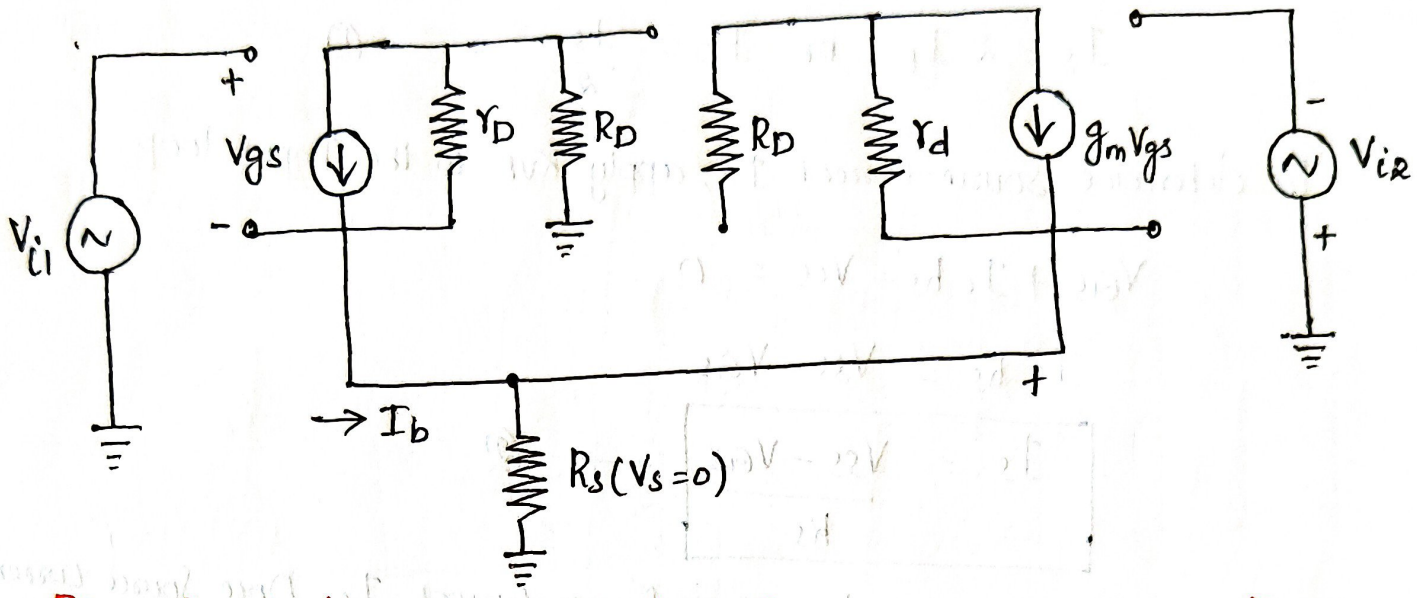
Ac Analysis is done by determining the Gain in both differential-Mode and Common-Mode

i) DIFFERENTIAL-MODE GAIN

The Ac Mode of a differential Amplifier operated in differential mode is shown in fig. 3

- Let $V_{i1} = V_{i2}$. Since there are two Inputs, the Analysis is Carried out by applying Superposition theorem.
- Since $V_{i1} = -V_{i2}$, $I_{D1} = -I_{D2}$ and hence Current flowing through Source Resistance R_S for every cycle is Zero.

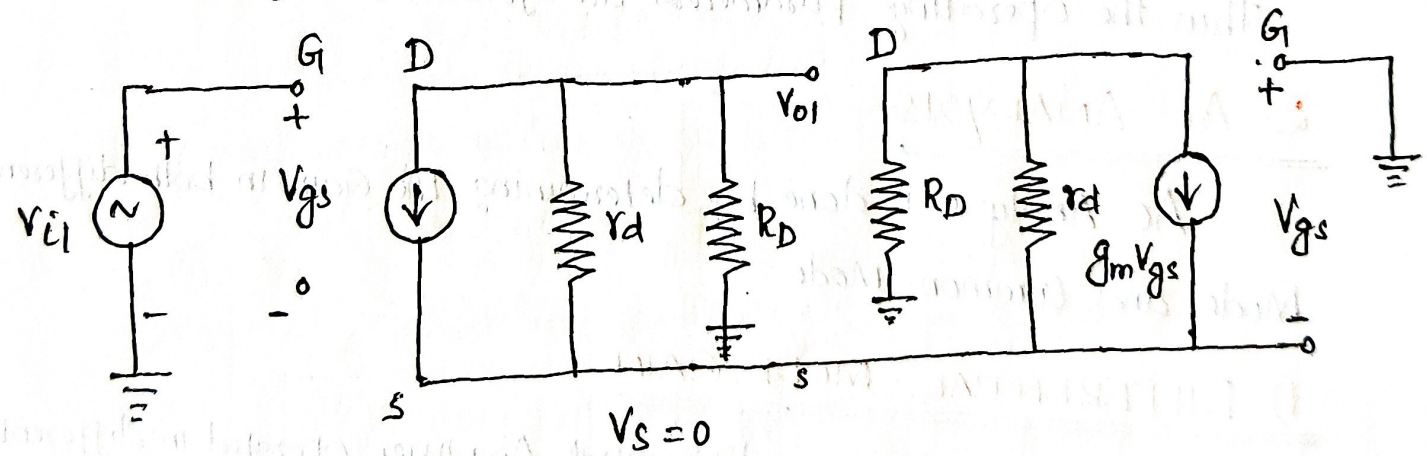
Therefore, Source Resistance R_s is considered open circuit of Gain in "differential Mode".



Fig·1. Small signal Model of dual Input Unbalanced output FET differential Amplifier.

Now Let us analyse the circuit by making $V_{DD} = -V_{SS} = 0$ and replacing the devices by their A.C Model. Since we are applying Super-position Theorem.

— Let us Consider V_{i1} and make $V_{i2} = 0$ and determine the Corresponding Output V_{o1}. The fig·2 is reduced to fig·2.



Fig·2. Small Signal Model of dual Input Balanced Output FET differential Amplifier with $V_{i2} = 0$

$$V_{o1} = I_o (R_D \| r_d)$$
$$= -I_d (R_D \| r_d)$$
$$= -g_m V_{gs} (R_D \| r_d)$$

Since $V_{gs} = V_{i1}$

$$\boxed{V_{o1} = -g_m V_{i1} (R_D \| r_d)}$$

Now consider V_{i2} and make $V_{i1} = 0$ and determine the corresponding output V_{o1}. The figure-2 is reduced to fig.3

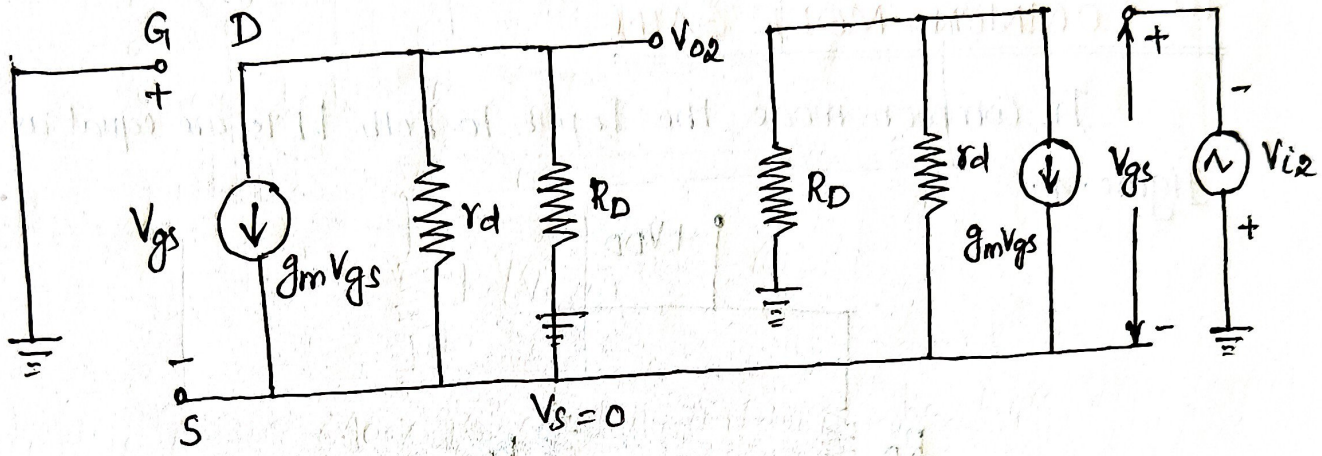


Fig.3

$$V_{o2} = I_o (R_D \| r_d)$$
$$= -I_o (R_D \| r_d)$$
$$= -(-g_m V_{gs})(R_D \| r_d)$$

Since $V_{gs} = V_{i2}$

$$\boxed{V_{o2} = g_m V_{i2} (R_D \| r_d)}$$

The overall output is sum of individual outputs

$$V_o = V_{o1} + V_{o2}$$
$$= -g_m V_{i1} (R_D \| r_d) + g_m V_{i2} (R_D \| r_d)$$

$$\boxed{V_o = g_m (R_D \| r_d)(V_{i2} - V_{i1})}$$

Where $(V_{i2} - V_{i1})$ is the differential input

Hence the differential Gain Ad is

$$A_d = \frac{V_o}{V_{i2} - V_{i1}} = \frac{g_m (R_D \| r_d)(V_{i2} - V_{i1})}{V_{i2} - V_{i1}} = g_m (R_D \| r_d)$$

$$A_d = g_m (R_D \parallel r_d)$$

If $r_d \geq 10 R_D$

$$A_d = g_m R_D$$

ii) COMMON-MODE GAIN

In common-mode, the Input to both FETs are equal as shown in figure 4.

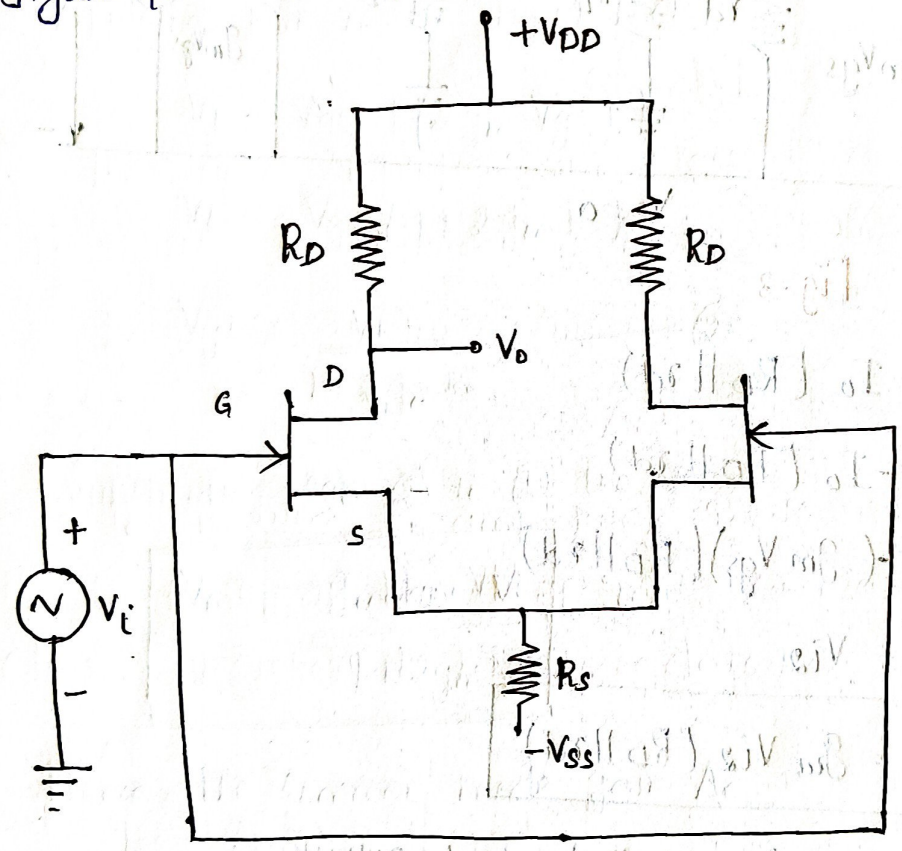


Fig.4. Common-mode Configuration

Hence $V_{i1} = V_{i2} = V_i$. The A.C model is drawn as shown in fig.5.

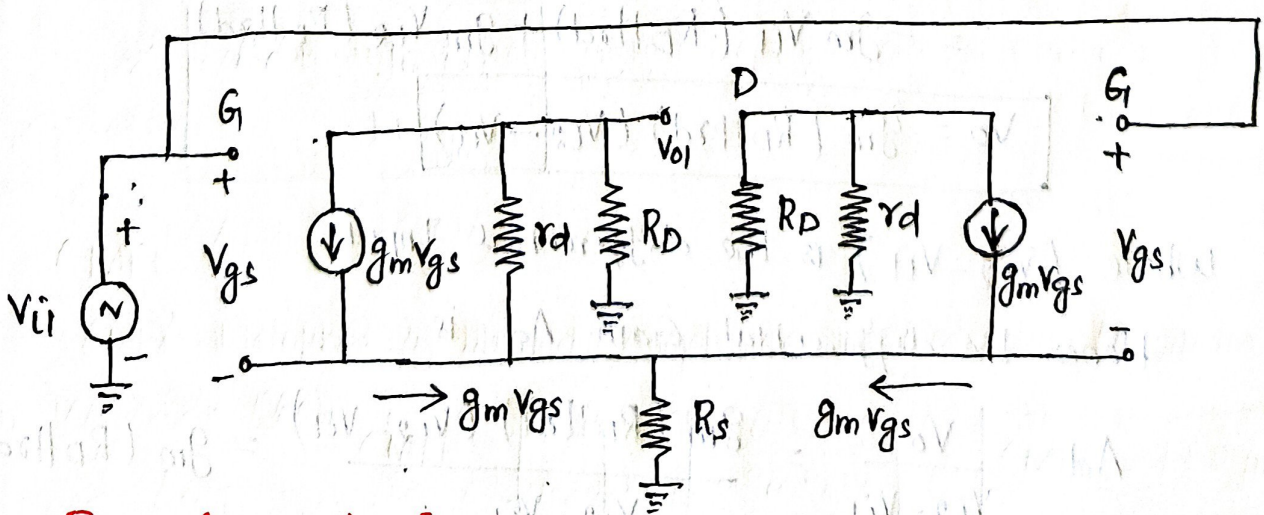


Fig.5. A.C Model for Common mode Configuration.

Since both the inputs are same, $I_{D1} = I_{D2} = I_D$. Hence current flowing through Source Resistance R_S gets added and $I_S = 2I_D$.

$$V_o = I_o (R_D \| r_d)$$

$$= -I_D (R_D \| r_d)$$

$$V_o = -g_m V_{gs} (R_D \| r_d)$$

If $r_d \geq 10 R_D$, then $\boxed{V_o = -g_m V_{gs} \cdot R_D}$ ——①

Applying KVL to the Input Loop.

$$V_i = V_{gs} + (2g_m V_{gs}) R_S$$

$$V_i = V_{gs} (1 + 2g_m R_S)$$

$$V_{gs} = \frac{V_i}{1+2g_m R_S}$$ ——②

Substituting eqn ② in ① we get

$$\boxed{V_o = \frac{-g_m R_D V_i}{1+2g_m R_S}}$$

Hence, the common mode gain A_c is

$$A_c = \frac{V_o}{V_i} = \frac{-g_m R_D V_i}{(1+2g_m R_S) V_i}$$

$$\boxed{A_c = \frac{-g_m R_D}{1+2g_m R_S}}$$

CMRR

CMRR is defined as the Ratio of differential-mode Gain (A_d) to the common-mode gain (A_c)

$$CMRR = \left| \frac{A_d}{A_c} \right| = \left| \frac{g_m R_D}{\frac{-g_m R_D}{1+2g_m R_S}} \right| \quad \therefore \boxed{CMRR = 1 + 2g_m R_S}$$

TUNED AMPLIFIERS

In order to obtained a large Overall Voltage gain, it is required to use a number of tuned amplifier stages in cascade.

- These cascaded Tuned Amplifiers are classified as

i) Single Tuned Amplifiers

ii) Double Tuned Amplifiers

iii) Stagger Tuned Amplifiers.

TYPES OF TUNED AMPLIFIERS

The Tuned Amplifiers are classified as

1. Small Signal Tuned Amplifiers
2. Large Signal Tuned Amplifiers.

1. SMALL SIGNAL TUNED AMPLIFIERS

- This is used for amplifying small signals at Radio Frequencies. The small signals have very small power and they are operated in class 'A' amplifiers to minimize distortion.

2. LARGE SIGNAL TUNED AMPLIFIERS

- These Amplifiers amplify the large signals at Radio frequencies. The Large signals have large Amount of power, hence they are operated in Class 'AB', 'B' or 'C' amplifiers.

* The Circuit efficiency will be high and it eliminates harmonic distortion.

SMALL SIGNAL TUNED AMPLIFIERS

A Number of Tuned Amplifier Stages are Connected together in Cascade so that large Voltage gain can be obtained. These Tuned Amplifiers are classified as

1. SINGLE TUNED AMPLIFIER

It uses only one parallel circuit as the load Impedance in each stage.

- All the tuned circuits are tuned to the same Frequency.

2. DOUBLE TUNED AMPLIFIER

It uses two Inductively Coupled Tuned circuits for each stage and all the tuned circuits are tuned to the same Frequency.

3. STAGGER TUNED AMPLIFIER

- In this method, a Number of single Tuned stages are connected in Cascade.

The Successive Tuned Circuits are tuned to slightly different frequencies.

SINGLE TUNED AMPLIFIERS

These Amplifiers use only one parallel circuit. With all Tuned Circuits tuned to the same Frequency.

- Single Tuned Amplifiers are of two types

1. Capacitance Coupled Single Tuned Amplifiers
2. Inductance Coupled Amplifiers.

1. CAPACITANCE COUPLED SINGLE TUNED AMPLIFIERS

The Output across the Tuned Circuit is Coupled to the Next Stage through the Coupling Capacitor. Hence it is called Capacitively Coupled Tuned Amplifiers.

CONSTRUCTION :

Fig. 1 shows the Circuit diagram of a capacitance coupled single Tuned Amplifier.

The tuned circuit is formed by LC circuit. The capacitance and Inductance values are selected such that the frequency to be amplified is equal to the Resonant Frequency.

* The Resistors R_1, R_2, and R_E are called 'Biasing Resistors'. These provide the operating current and voltage to the Transistors.

OPERATION :

A Radio Frequency signal, which is to be amplified, it is applied to the input of the Amplifier.

- The capacitance and Inductance values are adjusted such that the Resonant frequency is made equal to the Frequency of Input signal.

* When the frequency of the tuned circuit becomes same as that of the Input signal, then Resonance occurs. Hence large output signal appear across the Output.

- Thus the signal with frequency equal to the Resonant Frequency will be amplified and all the other frequency will be rejected by tuned circuit.

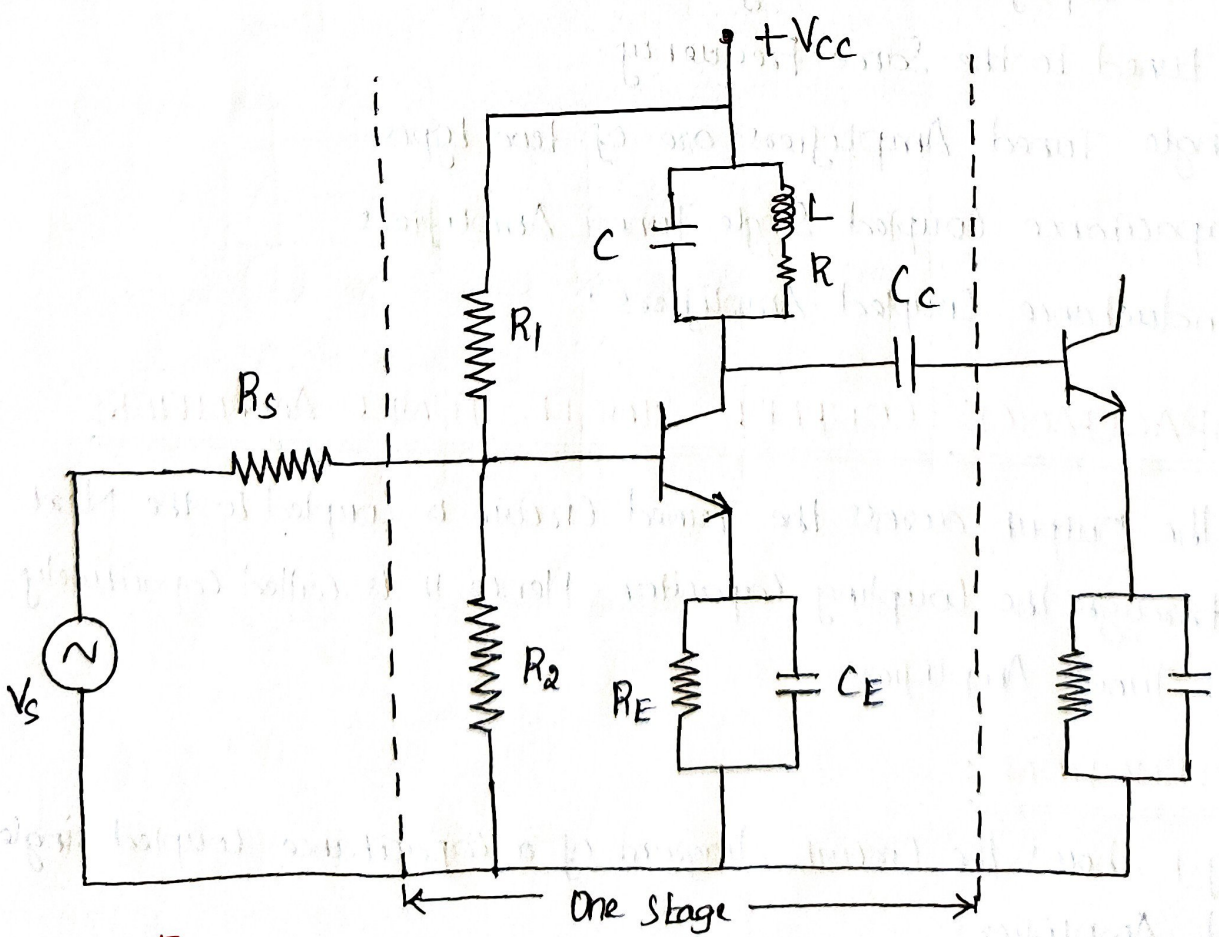


Fig. 1. Single Tuned Amplifier.

In the Single Tuned Amplifier, the output across the tuned circuit is coupled to the next stage through the coupling capacitor C_c as shown in fig. 1.

- Fig. 1 gives the equivalent circuit for the amplifier using high frequency hybrid Π model for the Transistor. In this circuit, R_i is the Input Resistance of the Next Stage.

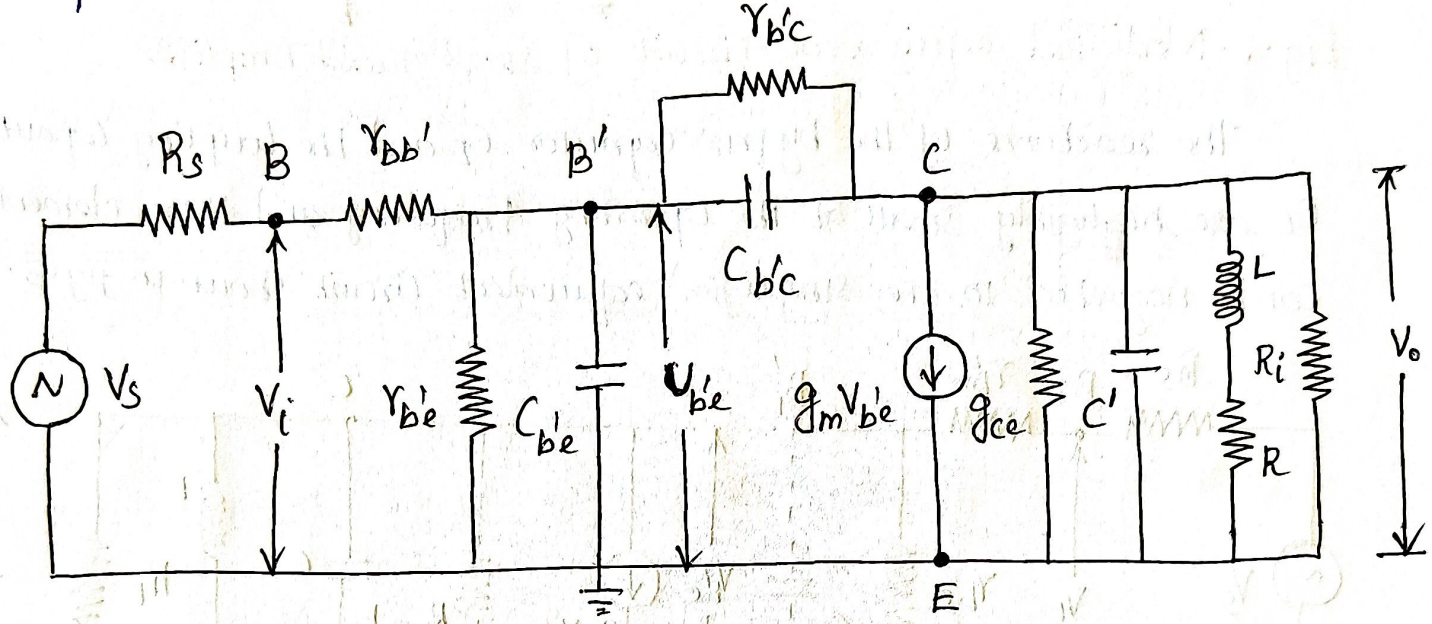


Fig. 1. Equivalent Circuit of Single Tuned Amplifier.

The equivalent circuit can be simplified where all the capacitance in the input circuit can be grouped together to form C_s is given by.

$$C_s = C_{b'e} + C_1 + C_{b'c}(1-A)$$

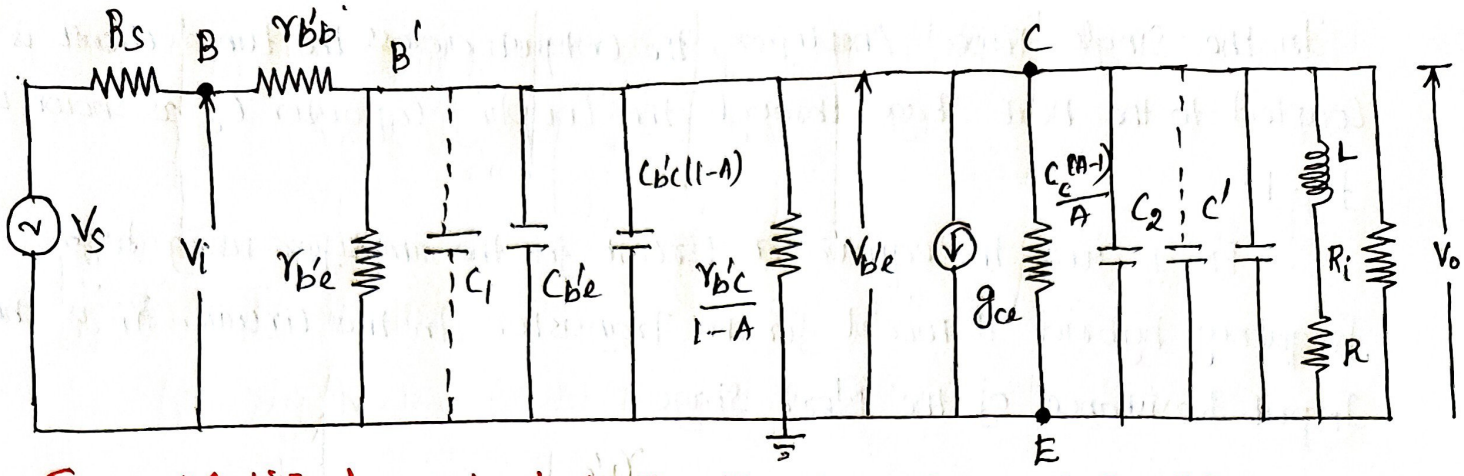
Similarly all the capacitances in the output circuit can be grouped together to form C' is given by

$$C = C_{b'c}\left(\frac{A-1}{A}\right) + C_2 + C'$$

Further, as simplified earlier,

$$g_{ce} = \frac{1}{r_{ce}} = h_{oe} - g_m h_{re} \simeq h_{oe} = \frac{1}{R_o}.$$

Where, R_o is the output Resistance of Current generator $g_m V_{b'e}$.



Fig·2· Modified equivalent Circuit of Single Tuned Amplifier

The reactance of the bypass capacitor C_E and the coupling capacitor C_C are negligibly small at the operating Frequency and these elements can be neglected in the simplified equivalent circuit shown in fig·3·

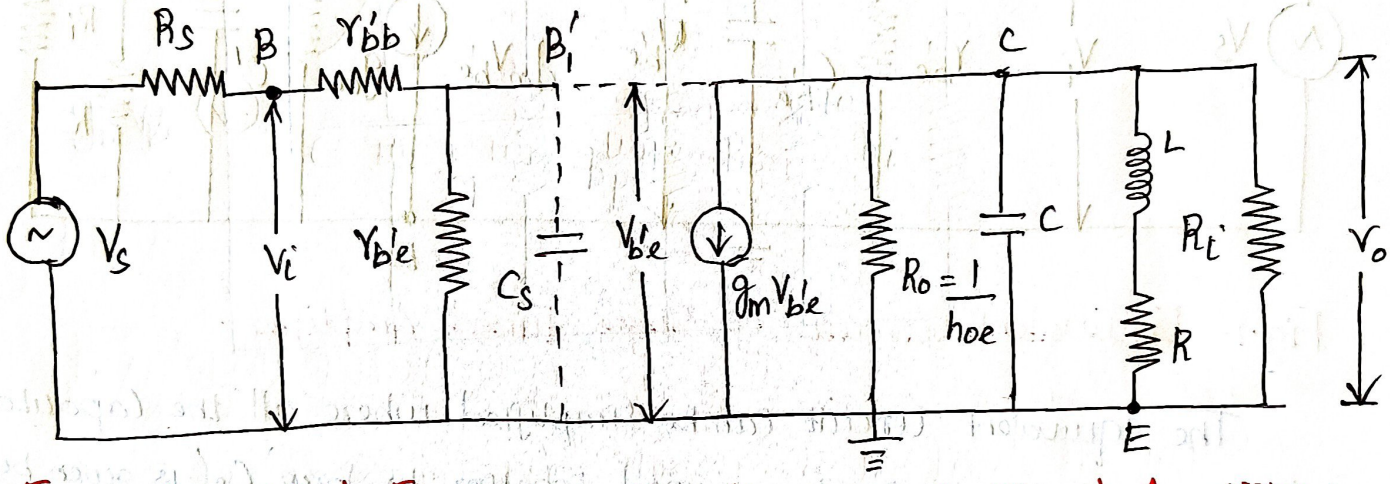


Fig. 3· Simplified Equivalent Circuit of Single Tuned Amplifier·

The admittance of the Inductor along with Resistor R is given by·

$$Y_i = \frac{1}{R+j\omega L} = \frac{1}{(R+j\omega L)} \cdot \frac{(R-j\omega L)}{(R-j\omega L)}$$

$$= \frac{R-j\omega L}{(R^2+\omega^2 L^2)}$$

$$= \frac{R}{R^2+\omega^2 L^2} - j\frac{\omega L}{R^2+\omega^2 L^2} \quad \text{——(1)}$$

$$Y = \frac{1}{R_p} + \frac{1}{j\omega L_p} \quad \text{——(2)}$$

Compare the equations (1) and (2) we get,

$$R_p = \frac{R^2 + \omega^2 L^2}{R} \quad \text{and} \quad L_p = \frac{R^2 + \omega^2 L^2}{\omega^2 L}$$

Thus, the Inductor branch may be represented by a Resistor R_p and Inductor L_p in Shunt.

- Quality Factor 'Q' of the coil at Resonance is given by

$$Q_0 = \frac{\omega_0 L}{R}$$

The output circuit of the Amplifier can be modified as shown in fig. 4

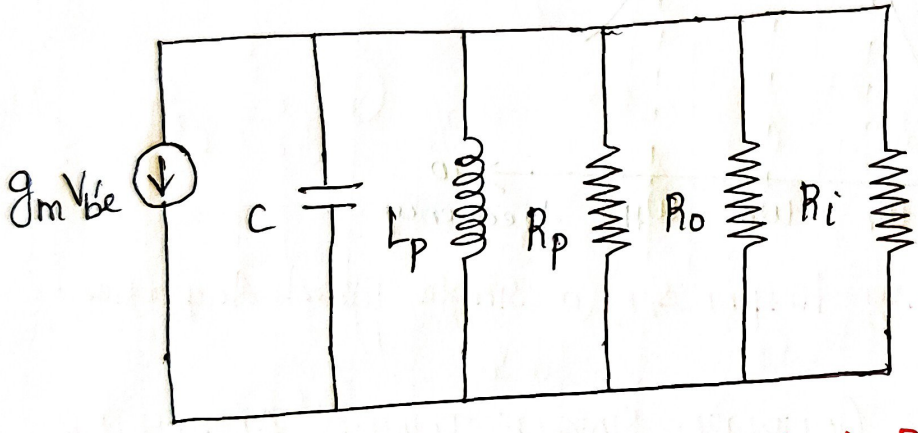


Fig. 4. Equivalent Circuit of the Output part of the Tuned Amplifier

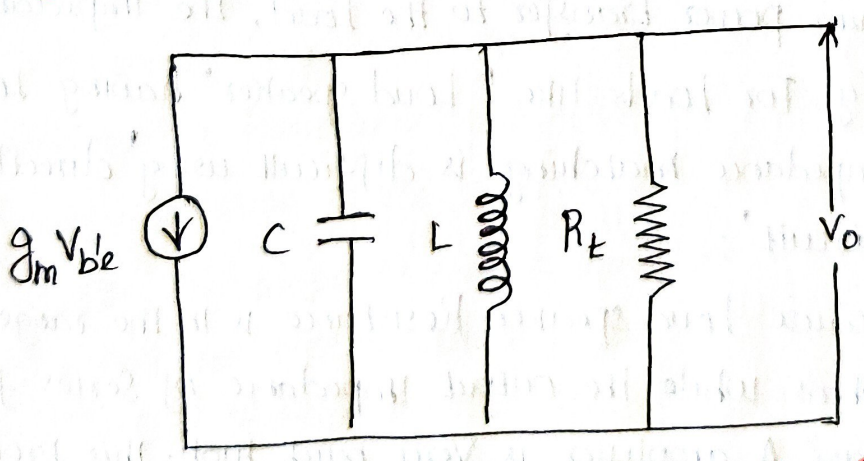


Fig. 5. Simplified Output Circuit of the Tuned Amplifier.

$$V_o = -g_m V_{b'e} Z.$$

$$V_{b'e} = V_i \frac{r_{b'e}}{r_{b'b} + r_{b'e}}$$

$$\therefore \quad V_o = -g_m \left(V_i \frac{r_{b'e}}{r_{b'b} + r_{b'e}} \right) Z$$

Hence, Voltage gain without considering the Source Resistance is given by

$$A = \frac{V_o}{V_i} = -g_m \left(\frac{r_{b'e}}{r_{b'b} + r_{b'e}} \right) z$$

Fig. 6 shows the magnitude of relative gain A/A_{res} plotted against 'ω'

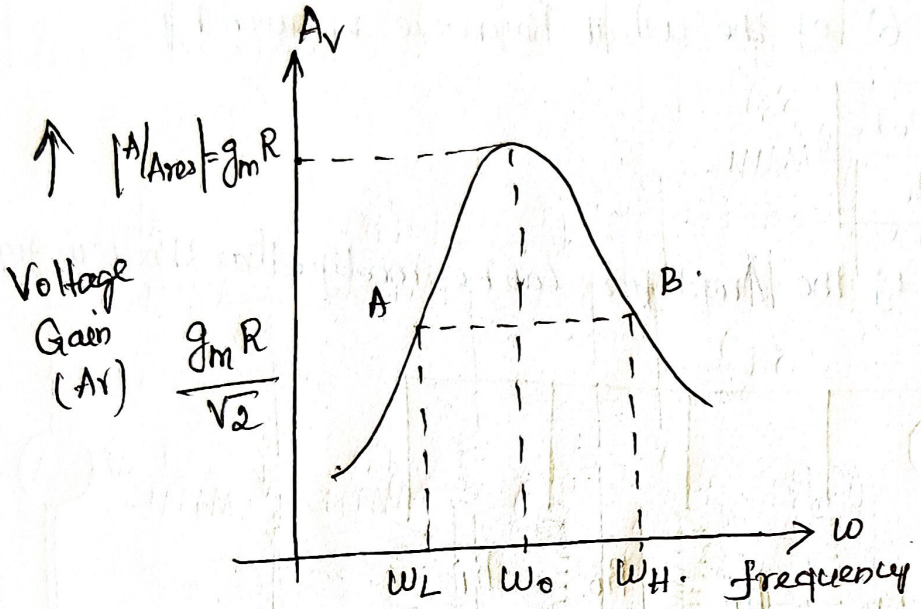


Fig. 6. Frequency Response of a Single Tuned Amplifier.

TRANSFORMER COUPLED SINGLE TUNED AMPLIFIER

For maximum power transfer to the Load, the impedance matching is necessary. For Loads like 'Loud speaker' having low impedance value, Impedance matching is difficult using 'directly Coupled Amplifier Circuit'.

- This is because Loud speaker Resistance is in the range of 3 to 4 ohms to 16 ohms while the output impedance of Series fed directly Coupled class A amplifier is Very much high. This problem can be eliminated by using a transformer to deliver power to the Load.

CIRCUIT DIAGRAM OF TRANSFORMER COUPLED AMPLIFIER

The basic Circuit of a transformer Coupled amplifier is shown in fig. 1. The Loud Speaker Connected to the Secondary acts as a Load having impedance of R_L ohms.

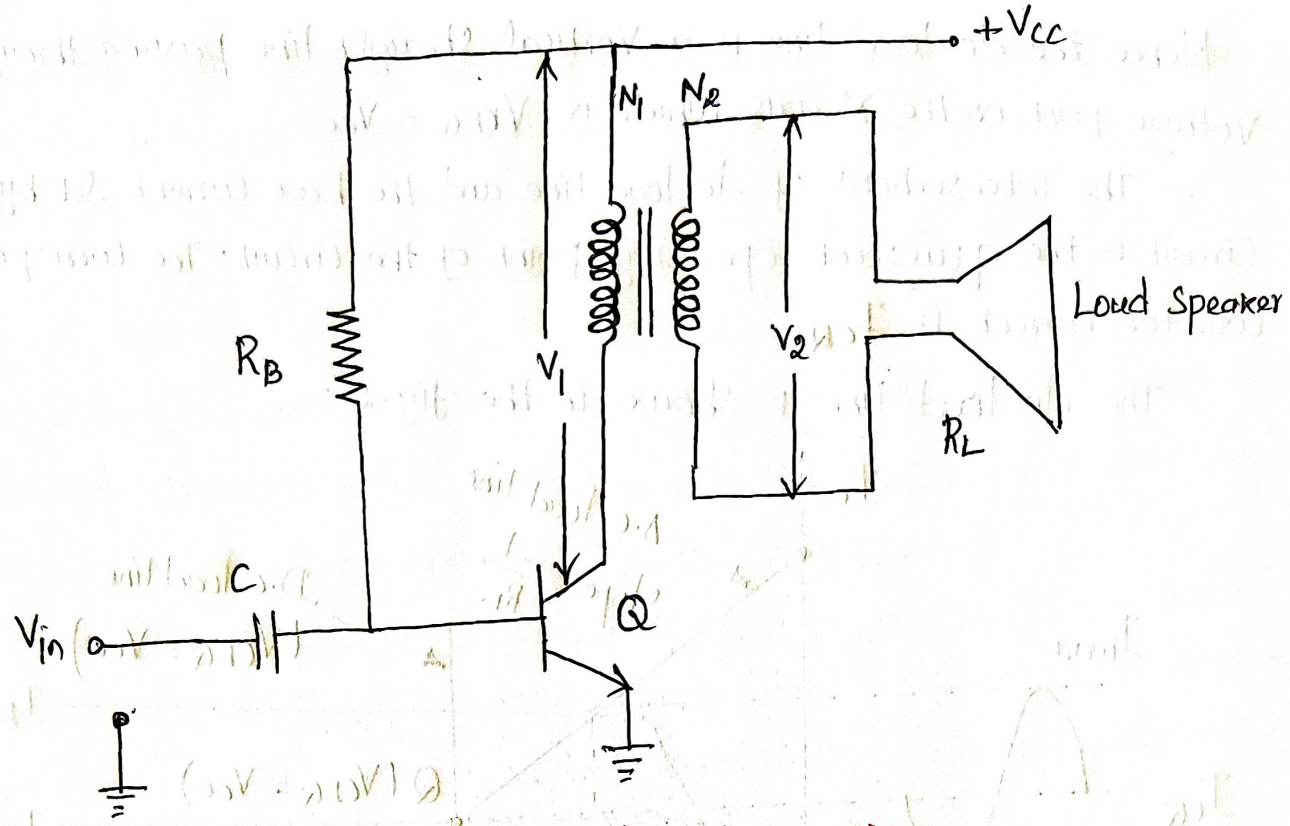


Fig.1. Transformer Coupled Class A amplifier.

The transformer used is a step down Transformer with turns ratio as

$$n = \frac{N_2}{N_1}$$

D.C OPERATION :

Assumed that the winding Resistance as Zero ohms. Hence for D.C Purposes, the Resistance is 0Ω. There is no dc voltage drop across the Primary winding of the transformer.

* The slope of the dc load line is reciprocal of the dc Resistance in the collector circuit, which is zero in this case. Hence slope of the dc load line is ideally infinite. This tells that the dc load line in the ideal condition is a vertically straight line.

Applying KVL to the collector circuit we get

$$V_{CC} - V_{CE} = 0$$

$$V_{CC} = V_{CE}$$

This is the dc bias voltage V_{CEQ} for the Transistor

$$V_{CEQ} = V_{CC}$$

Hence the dc load line is a vertical straight line passing through a voltage point on the X-axis which is $V_{CEQ} = V_{cc}$.

- The intersections of dc load line and the base current set by the circuit is the quiescent operating point of the circuit. The corresponding collector current is 'I_{CQ}'

The dc load line is shown in the fig. 2.

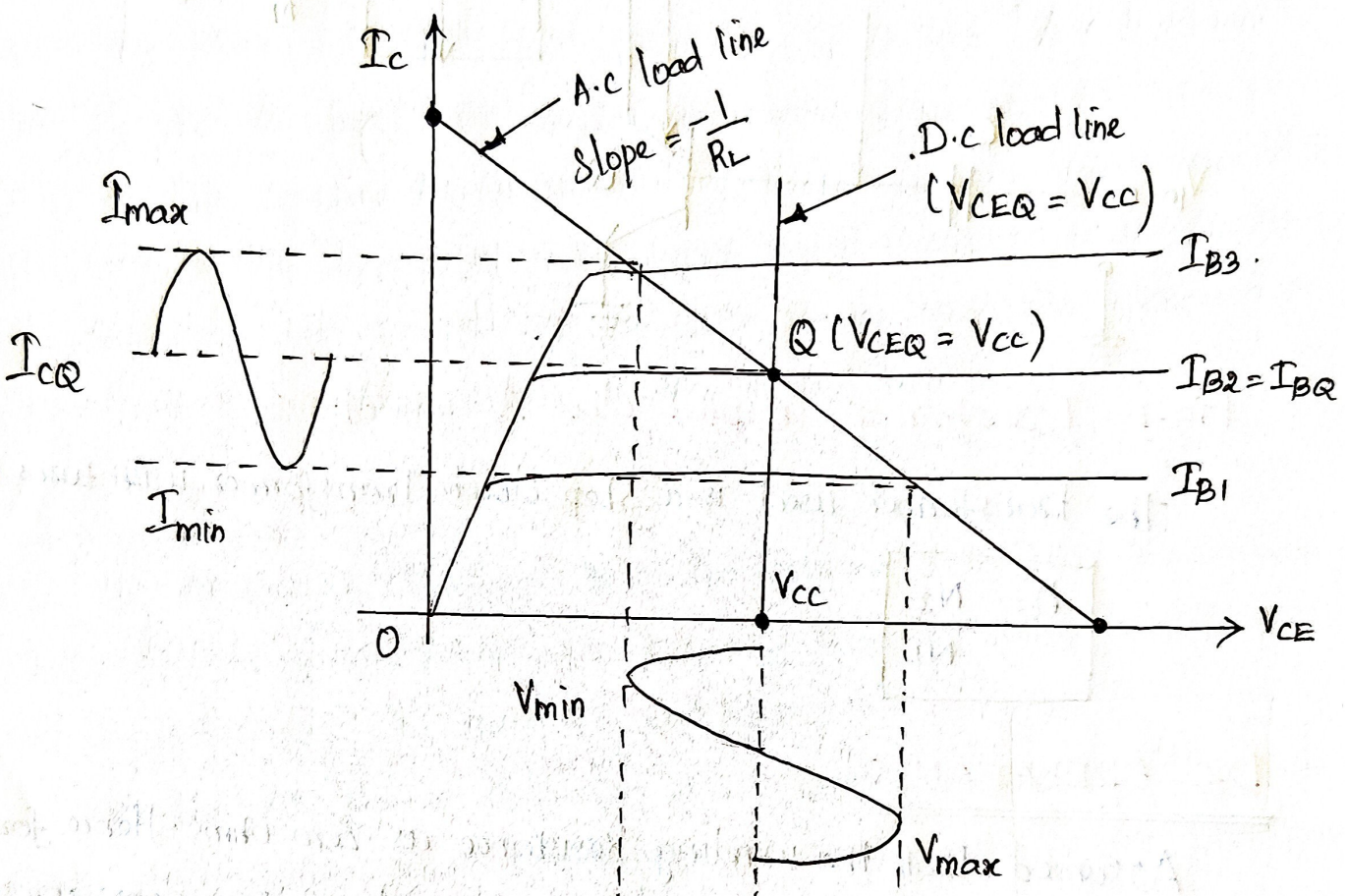


Fig. 2. Load lines for Transformer Coupled Class A amplifier

DC POWER INPUT :

The dc power input is provided by the supply voltage with no signal input, the dc current drawn is the collector bias current 'I_{CQ}'

- Hence the dc power input is given by

$$P_{DC} = V_{cc} I_{CQ}$$

AC OPERATION :

For the A.c Analysis, it is necessary to draw an Ac load line on the output characteristics.

For a.c purposes, the Load on the Secondary is the Load Impedance R_L ohms and the reflected load on the primary i.e, R_L can be calculated using the equation.

- Already, we know that $\boxed{R_L' = \frac{R_L}{n} = \left(\frac{N_1}{N_2}\right)^2 R_L}$

The load line drawn with a slope of $\left(\frac{-1}{R_L}\right)$ and passing through the operating point i.e, quiescent point 'Q' is called 'A.C load Line'. The dc and AC load lines are shown in the figure 2.

* The Output or Current i.e, Collector Current Varies around its quiescent Value I_{CQ}, when ac input signal is applied to the Amplifier. The Corresponding output Voltage also Varies sinusoidally around its quiescent Value V_{CEQ} which is V_{cc} in this case.

AC OUTPUT POWER

The AC power developed is on the primary side of the Transformer. While calculating this power, the primary Values of Voltage and Current and reflected load R_L must be considered.

* The AC power delivered to the Load is on the Secondary side of the transformer while calculating load Voltage, Load Current, Load Power the Secondary Voltage, Current and R. Load R_L must be considered.

Let V_{im} - Magnitude or Peak Value of Primary Voltage

$V_{1\,rms}$ - R.M.S Value of Primary Voltage

I_{1m} - Peak Value of Primary Current

$I_{1\,rms}$ - R.M.S Value of Primary Current.

Hence, the AC power developed on the Primary is given by

$$P_{ac} = V_{1\,rms}\, I_{1\,rms}$$

$$P_{ac} = I_{1\,rms}^2\, R_L'$$

$$P_{ac} = \frac{V_{1\,rms}^2}{R_L'}$$

$$P_{ac} = \frac{V_{im}}{\sqrt{2}} \cdot \frac{I_{im}}{\sqrt{2}} = \frac{V_{im} I_{im}}{2}$$

$$P_{ac} = \frac{I_{im}^2 R_L'}{2}$$

$$\boxed{P_{ac} = \frac{V_{im}^2}{2 R_L'}}$$

Similarly the Ac power deliver to the Load on Secondary also can be Calculated using Secondary quantities:

V_{2m} - Magnitude or Peak Value of Secondary or Load Voltage

$V_{2\,rms}$ - R.M.S Value of Secondary or Load Voltage

I_{2m} - Magnitude or Peak Value of Secondary or Load Current

$I_{2\,rms}$ - R.M.S Value of Secondary or Load Current.

$$P_{ac} = V_{2rms} \cdot I_{2rms} = I_{2rms}^2 R_L' = \frac{V_{2rms}^2}{R_L}$$

$$P_{ac} = \frac{V_{2m} I_{2m}}{2} = \frac{I_{2rms}^2 R_L}{2} = \frac{V_{2m}^2}{2 R_L} \quad \therefore \boxed{P_{ac} = \frac{V_{2m}^2}{2 R_L}}$$

The power delivered on Primary is Same as power delivered to the Load on Secondary assuming ideal Transformer.

- The Slope of the ac load Line is

$$= \frac{1}{R_L'} = \frac{I_{im}}{V_{im}}$$

The generalized expression for AC Power output represented by

$$\boxed{P_{ac} = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8}}$$

EFFICIENCY :

$$\% \eta = \frac{P_{ac}}{P_{dc}} \times 100$$

$$\boxed{\% \eta = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8 V_{cc} I_{CQ}} \times 100}$$

DOUBLE TUNED VOLTAGE AMPLIFIER

To overcome the drawback of single Tuned Amplifier, double Tuned Amplifiers are used.

- In this method, two tuned circuits are inductively coupled to each other. Fig. 1 shows the circuit of a double Tuned Voltage Amplifier.

* L_1, C_1 is used as Collector Load and L_2 C_2 is used as Output Circuit. R_1, R_2, R_E Provide dc Current and Voltage for the Transistor.

• This Circuit Provides high impedance to the Input Signal and a large output appears across the Tuned Circuit L_1, C_1. This Output is Inductively Coupled to L_2 C_2 tuned Circuit

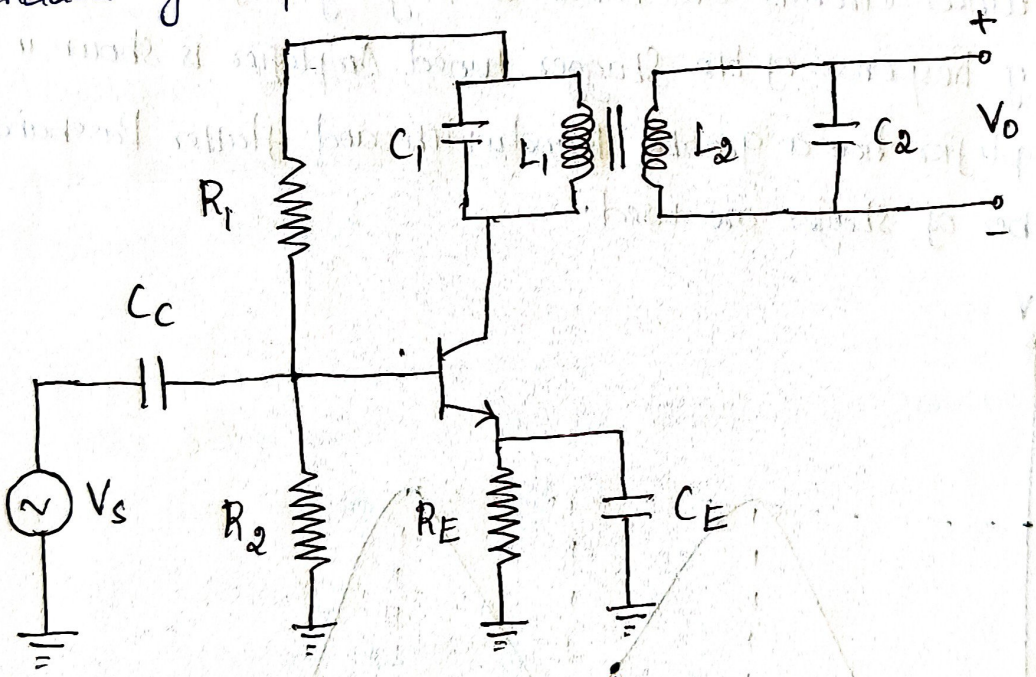


Fig. 1. Double Tuned Amplifier.

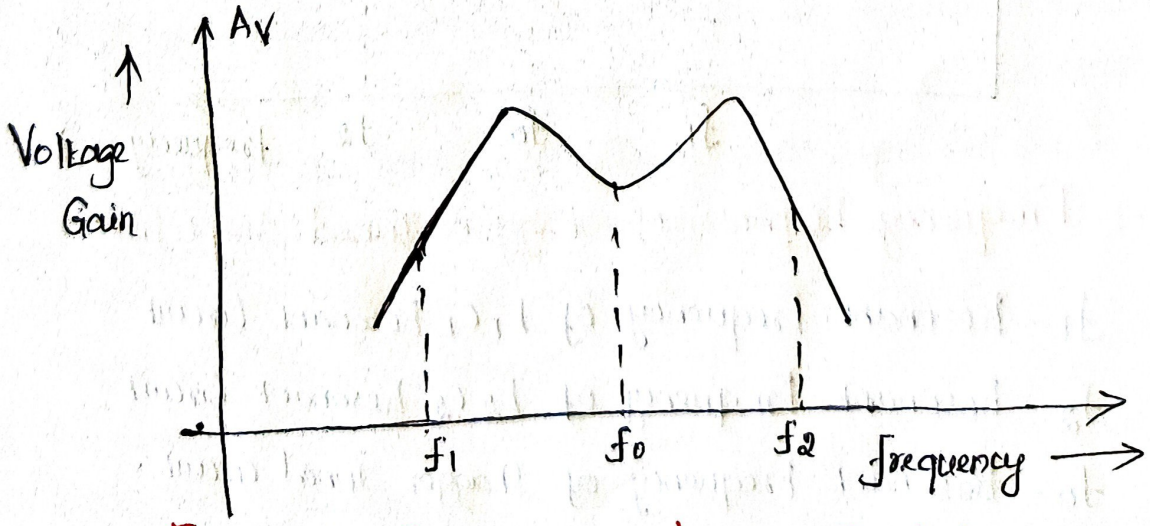


Fig. 2. Frequency Response of double Tuned Amplifier.

This is used in Radio and Television Receiver. The fig. 2 shows the Frequency Response of double Tuned Amplifier.

- This circuit provides high Selectivity, High Gain and Large Bandwidth.

STAGGER - TUNED AMPLIFIER

If two or more circuits are Synchronously tuned and Cascaded, the Overall Bandwidth will be decreased

- In Stagger Tuned Amplifiers, the Cascaded Circuits are tuned to Slightly different frequencies, then bandwidth will be increased. This technique is called 'Stagger Tuning'.

* The tuned Circuits are tuned to Slightly different frequencies. The Frequency Response of the Stagger tuned Amplifier is shown in fig. 1.

- This amplifier has a greater Bandwidth and flatter Passband, if more Number of Stages are used.

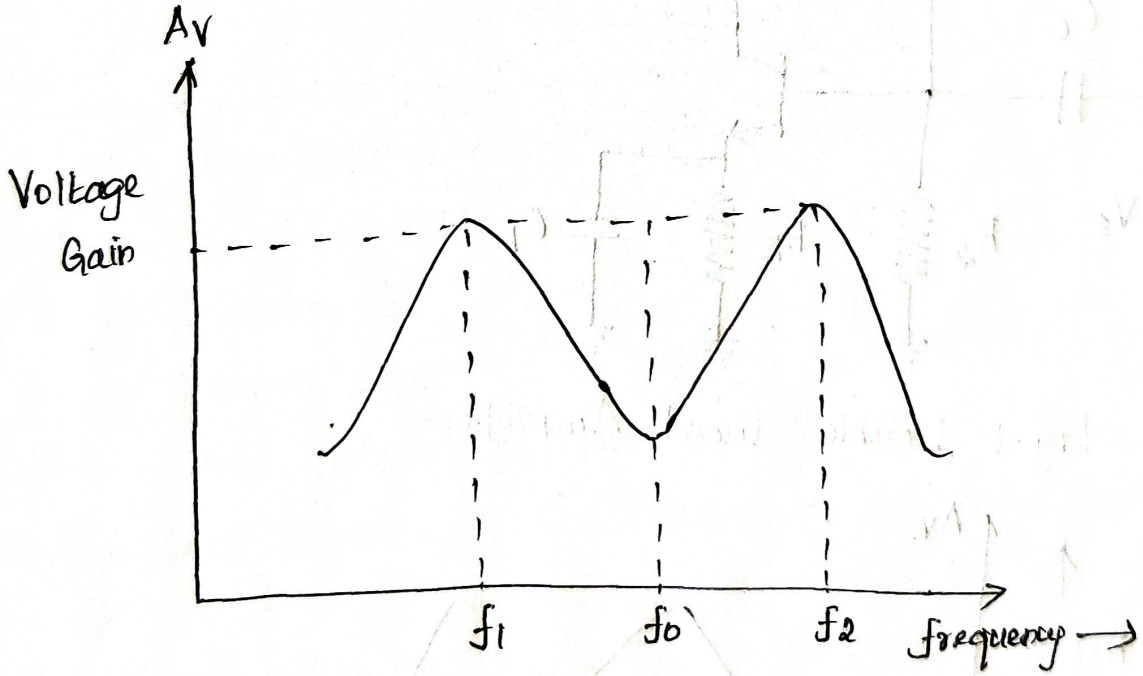


Fig. 1. Frequency Response of Stagger Tuned Amplifier.

f_1 - Resonant Frequency of $L_1 C_1$ Resonant Circuit

f_2 - Resonant Frequency of $L_2 C_2$ Resonant Circuit

f_o - Resonant Frequency of Stagger Tuned Circuit.

NEUTRALIZATION

The technique used for the elimination of Potential Oscillations is Called 'Neutralization'

NEED FOR NEUTRALIZATION

- In tuned Amplifiers, the transistors are used at Resonant Frequency to amplify the Narrow band of high Frequencies

* At this frequency, the Junction capacitance between Base and Collector of the transistor becomes dominant. Thus the Reactance of the circuit is Low.

- This reactance provides a positive feedback which causes Oscillations in the circuit and makes the system unstable.

* To prevent oscillations in Tuned Amplifiers, the Neutralization Technique is used.

NEUTRALIZATION METHODS

The Stage Gain Should be reduced to prevent Oscillations in the Circuit. This can be done by.

1. Reducing Q
2. Stagger Tuning
3. Loose Coupling between the stages

The Feedback signal can be cancelled by an Additional Feedback signal that is equal in Amplitude and opposite in phase i.e., a portion of Output Signal is Feedback to the Input with Same Amplitude but opposite phase. This is achieved using Neutralization.

- Neutralization can be done in three Methods.

1. Hazeltine Neutralization
2. Neytrodyne Neutralization
3. Rice Neutralization
4. Neutralization using Coil.

HAZELTINE NEUTRALIZATION METHOD

This is a Neutralization Technique employed in Tuned RF Amplifiers to maintain Stability.

- In the circuit shown in fig.1, the undesired effect of the collector to base capacitance of the transistor is neutralized by introducing a signal which cancels the signal coupled through the collector to Base Capacitance.

* Fig.1. Shows that a small Variable Capacitance C_N is connected from the bottom of the coil to the Base of the Transistor. The Neutralization Process is achieved by 'C_N'.

- It introduces a signal to the base of the Transistor such that is cancels out the signal fed to the Base by 'C_{be}'. Generally a Variable Capacitor is used for Neutralization as the value of 'C_{bc}' Changes with time.

* By Properly adjusting 'C_N', exact Neutralization is achieved

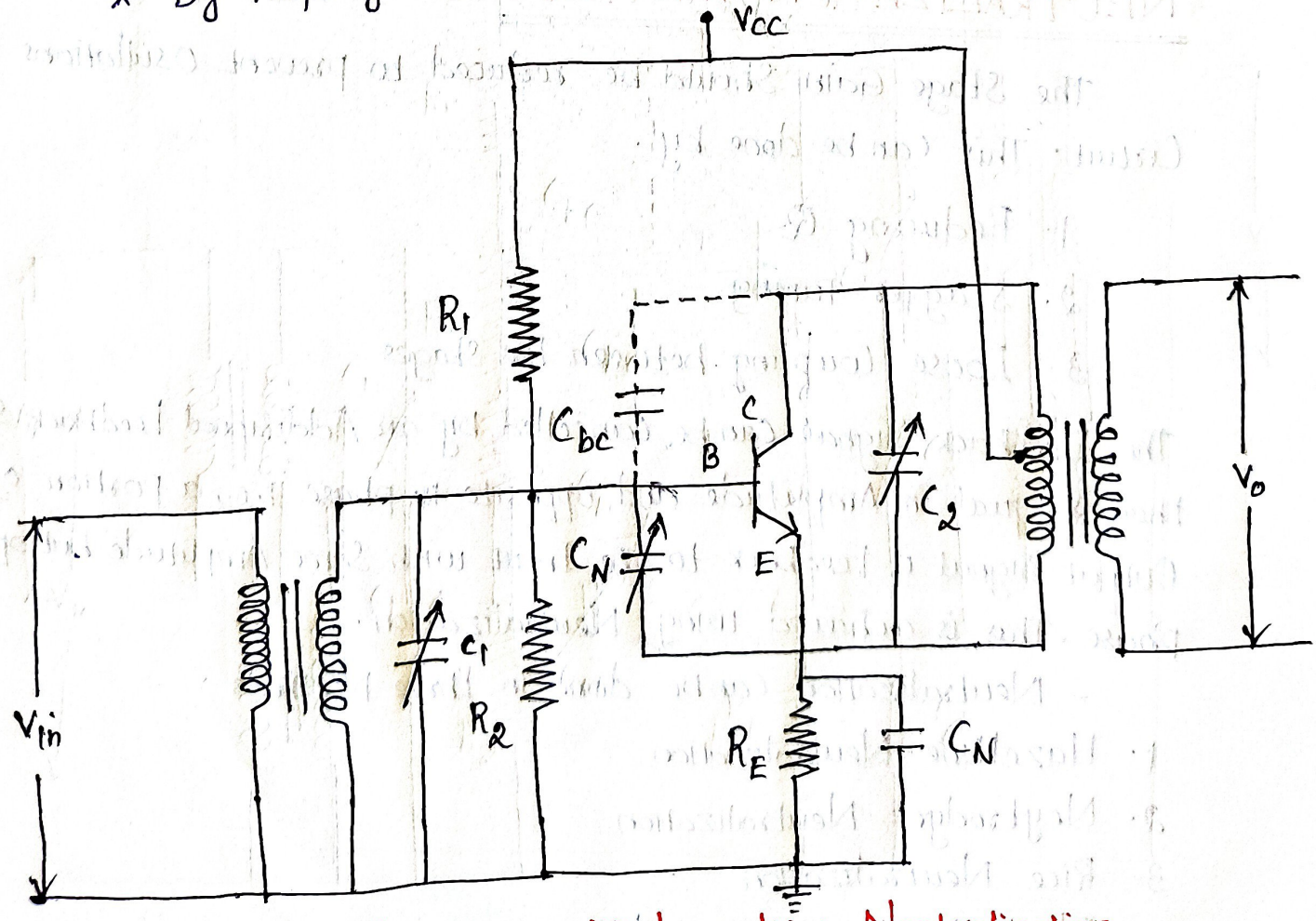


Fig.1. Tuned RF Amplifier with hazeltine Neutralization.

DRAWBACK

- The Capacitance Value changes with time. The Neutralizing Capacitor should be adjusted correctly to completely Neutralize the Internal Capacitance.

NEUTRODYNE NEUTRALIZATION

In the modified version of hazeltine Neutralization called 'Neutrodyne Neutralization' Technique.

- In this circuit, the Neutralization capacitor 'C_N' is connected from the lower end of the base coil of Next stage (ie Secondary coil) to the Base of the Transistor (B).

* Hence it is connected with V_{cc} which ensures that, it is insensitive to any variation in the supply voltage 'V_{cc}' and provides higher stabilization for the Tuned Amplifier

Fig.2 shows the Neutrodyne Neutralization circuit.

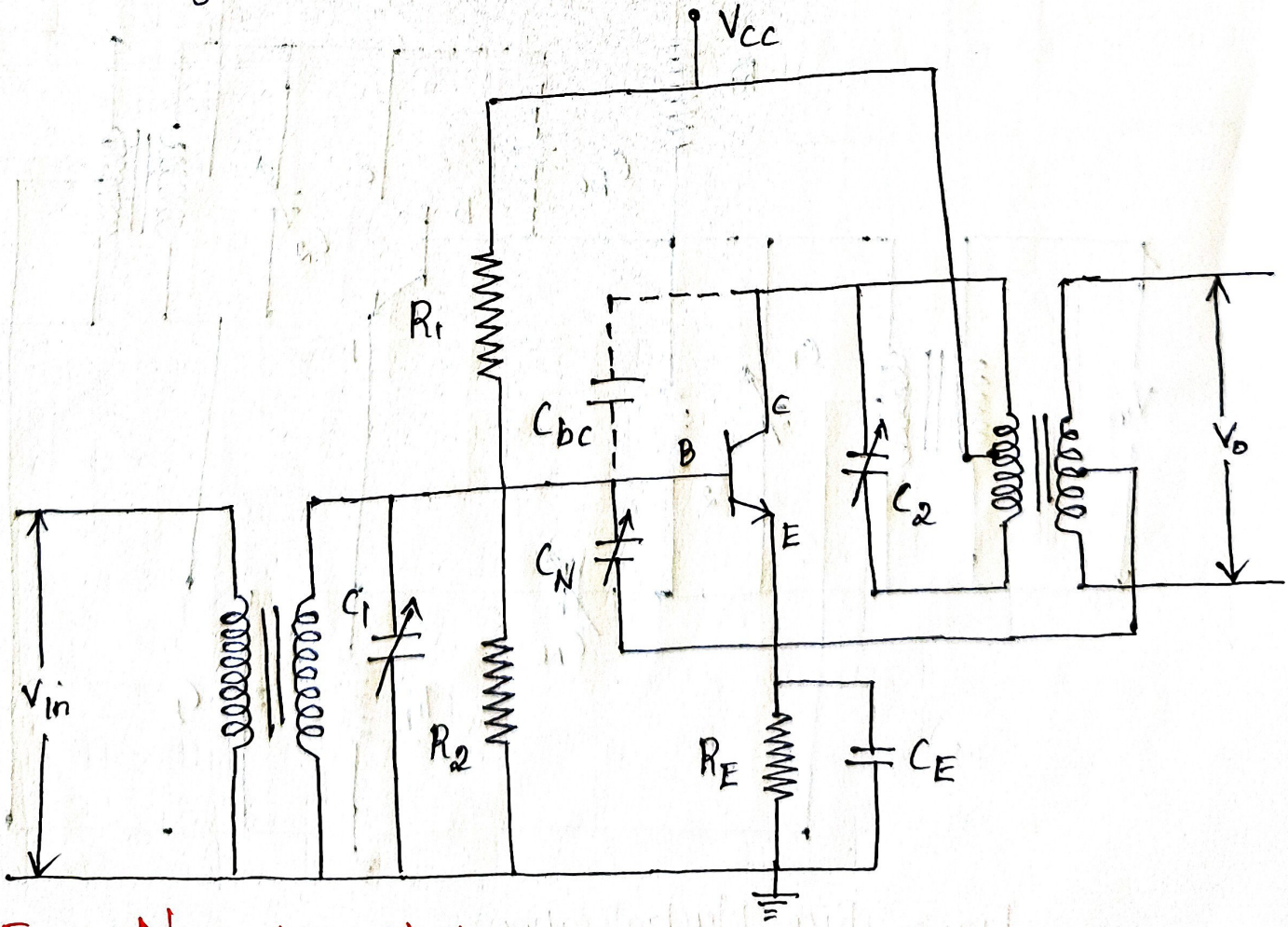


Fig.2. Neutrodyne Neutralization.

ADVANTAGES

1. The capacitor is insensitive to variations in V_{CC}
2. High stability.

RICE NEUTRALIZATION

Fig. 3 shows the Rice method of Neutralization and ~~it is equivalent Circuit is shown in fig. 4.~~

- Here the Required phase shift is obtained by means of tapping in the Base coil.

* When the equivalent Bridge circuit is properly balanced by adjustment of the coil tapping or by selecting a suitable value for C_N Neutralization is obtained.

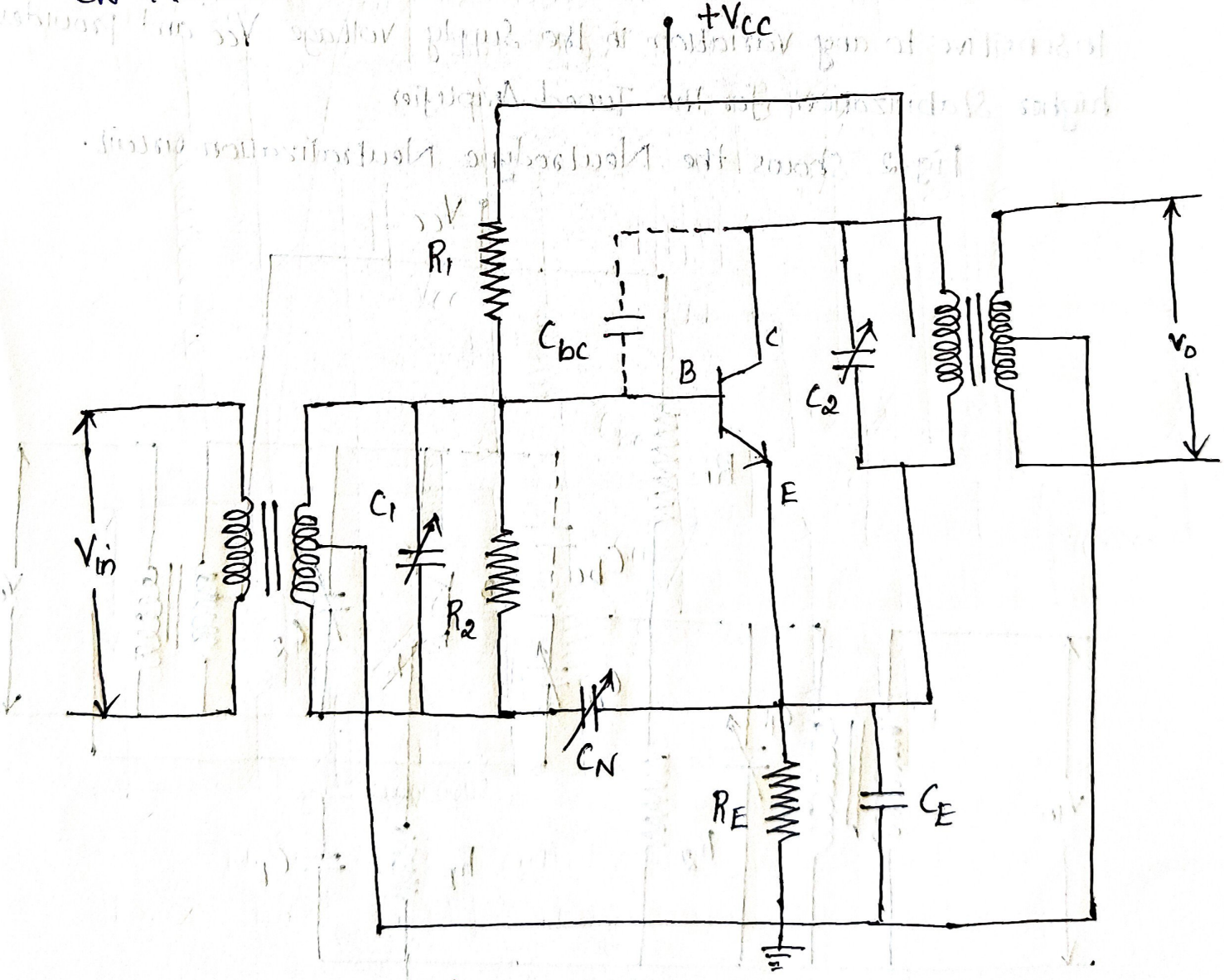


Fig. 3. Rice Neutralization.

NEUTRALIZATION USING COIL

Fig.4 shows coil Neutralization. In this method, we require phase shift to Neutralize the energy received by the Control base through Base Capacitance is achieved by feeding back energy through the feedback coil.

- Perfect Neutralization results at a frequency at which the Reactance of the Inductive branch equals the Reactance of the Base Capacitance.

* In this method, Part of the tuned circuit at the base of Next stage is used for minimum coupling to other windings

- It is made perpendicular to the Coupled windings. The Voltage across the Inductor will Cancel the feedback signal produced by the Collector Base Capacitance 'Cbc'

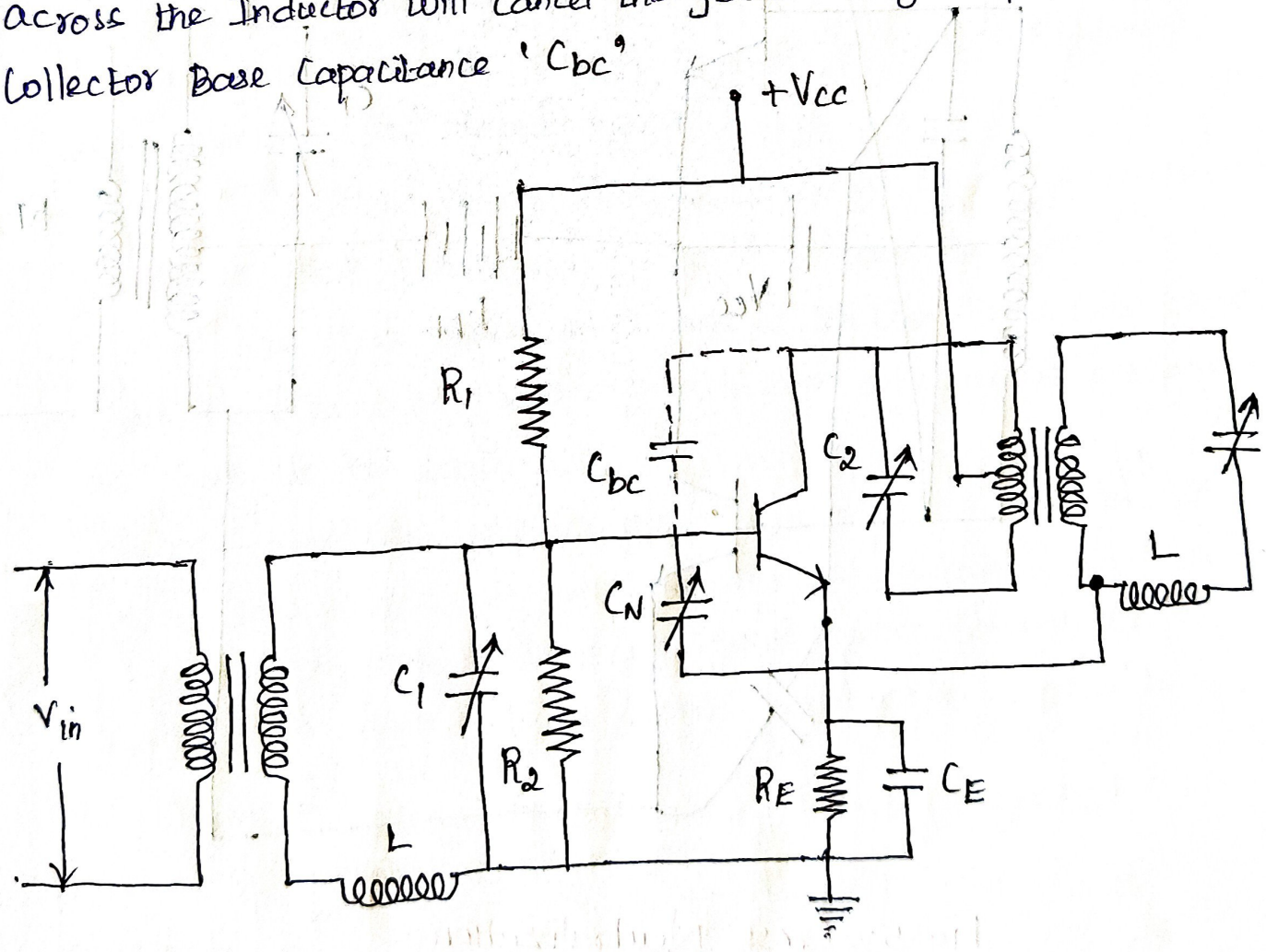


Fig.4. Tuned Amplifier using coil.

CROSS NEUTRALIZATION

When the power Amplifier comprises of two tubes connected in Push pull arrangement, Neutralization can be obtained by Cross feeding from one electrode to the other electrodes of the other as shown in fig.5.

- Such a method is termed as 'Cross Neutralization'

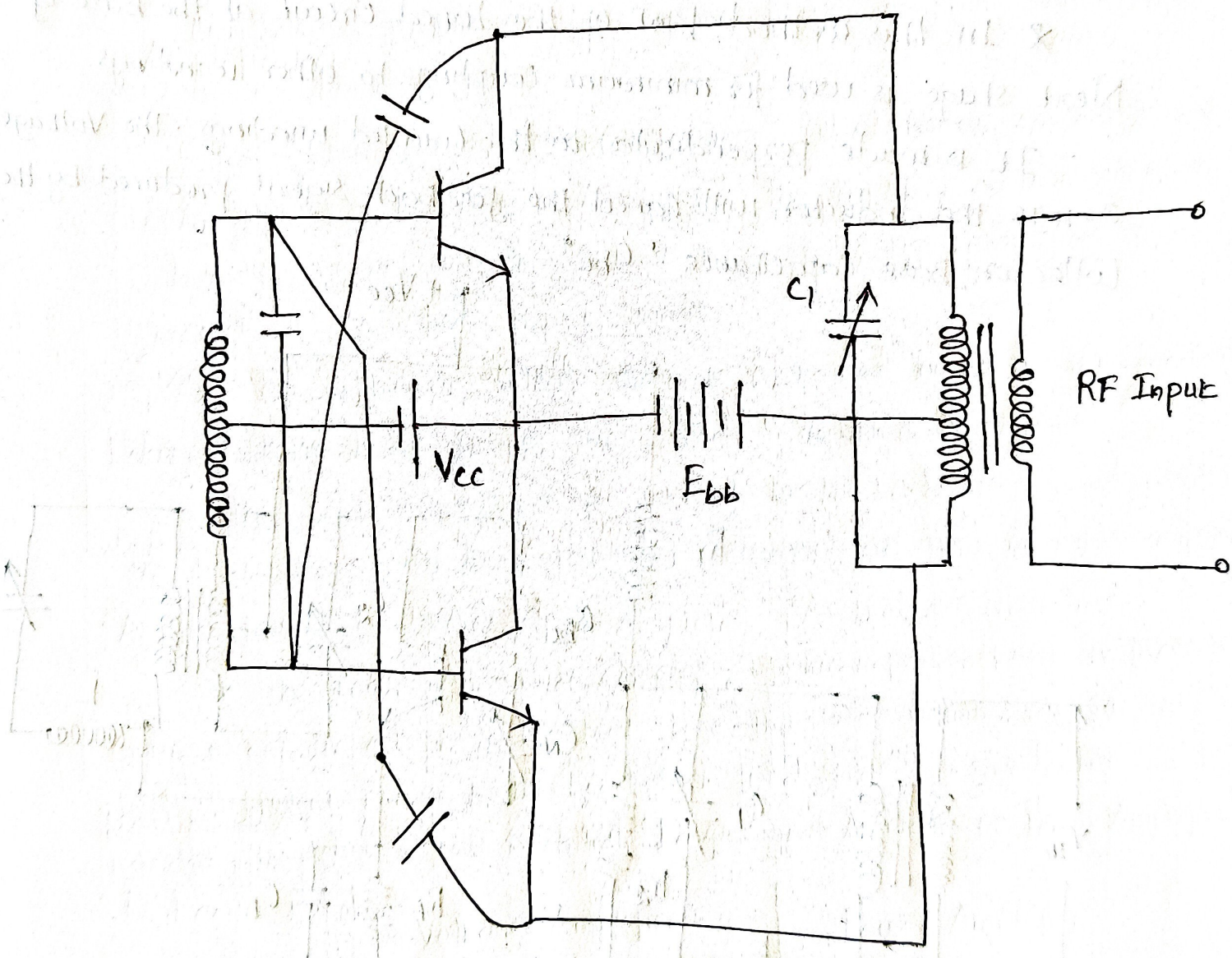


Fig.5. Cross Neutralization.

POWER AMPLIFIERS

The Voltage Amplifiers operate in the Linear portion of the Transfer Characteristics, Closer to Q-point of the Amplifier. These amplifiers are Called 'Small Signal Amplifiers'

– Because they are mainly used for Voltage Amplification but not used for providing large power to the Loads.

POWER AMPLIFIER SYSTEM

Consider a public address system power Amplifier (or) amplifying System as shown in fig.1.

– The System Consists of many stages Connected in Cascade. Hence Basically it is a 'multistage Amplifier'. The Input is Sound signal of a human Speaker and the Output is given to the Loud speaker which is an amplified Input signal

* The Sufficient Voltage Gain is Obtained by all the Intermediate Stages. Hence these stages are Called 'Voltage Amplifiers'

– The Last stage gives an Output to the Load like a Loud speaker. The Last stage must be Capable of delivering an appreciatable amount of ac power to the Load.

* The main Aim is to develop Sufficient power hence the Voltage Gain is not important in the Last stage. This stage which develops and feeds Sufficient power to the Load, like loud speaker, Servo motor, handling the large signals is Called 'Large Signal Amplifier or Power Amplifier'.

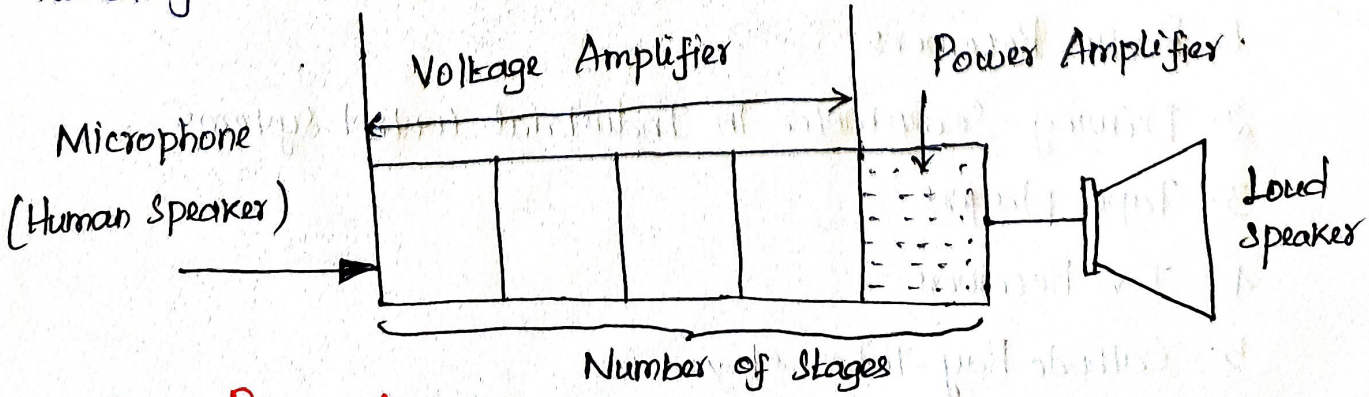


Fig.1. Power Amplifier System

COMPARISON BETWEEN VOLTAGE AND POWER AMPLIFIER

The Voltage Amplifiers gives an increased Voltage Output to a high Resistance Load.

- The power Amplifiers produces an increase in Output power to a relatively low Resistance Load.

Table.1. Comparison of Voltage and Power Amplifier.

Parameter	Voltage Amplifiers	Power Amplifiers
Amplification	Voltage	Current (or) power
Current Gain	Large ($\sim$100)	Between 20 and 50
Input Impedance	Lesser than its Output Impedance	Larger compared to the Output Impedance
Size	Small	Bulky
Power handling	Low	High
Inter-stage	RC Coupling	Transformer Coupling
Applications	As a pre-Amplifier or Voltage Amplifier	As the Last stage in Public Address system, TV, Radio Receiver and other Circuits

POWER AMPLIFIER APPLICATIONS

1. Radio Receivers
2. Driving Servomotor in Industrial control systems
3. Tape players
4. T.V. Receivers
5. Cathode Ray Tubes etc,

CLASSIFICATION OF POWER AMPLIFIERS

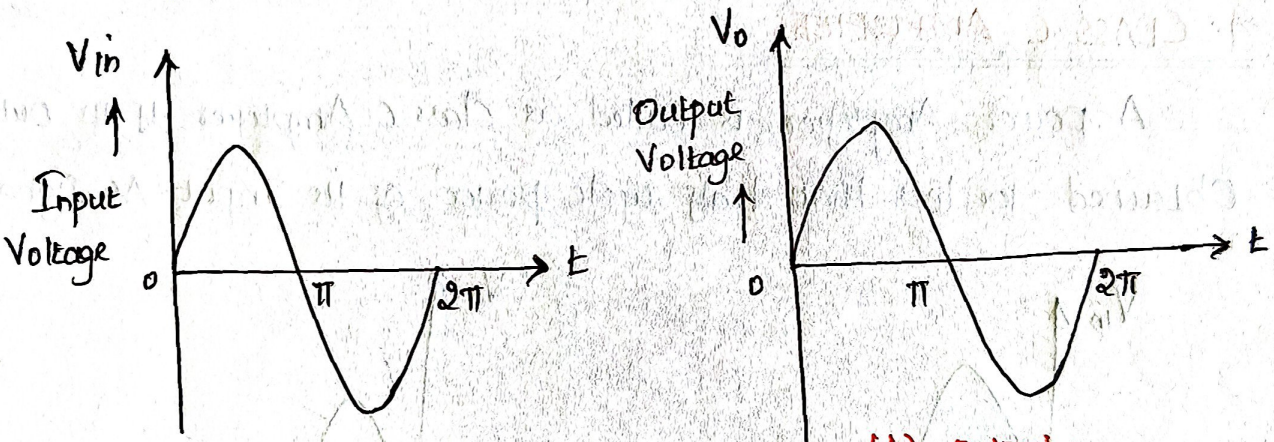
The power Amplifiers are classified based on the position of Q-point on the Load line.

– Depending upon the transistors biasing and the Amplitude of the Input Signal, the transistor Conducts during the specified portion of the Cycle.

* The power Amplifiers are classified as Class A, B, C, AB and D amplifiers

1. CLASS A AMPLIFIER

The transistor Conducts for the complete cycle of the AC input i.e, 360°. So, the output Current flows for the full cycle of the AC Input.

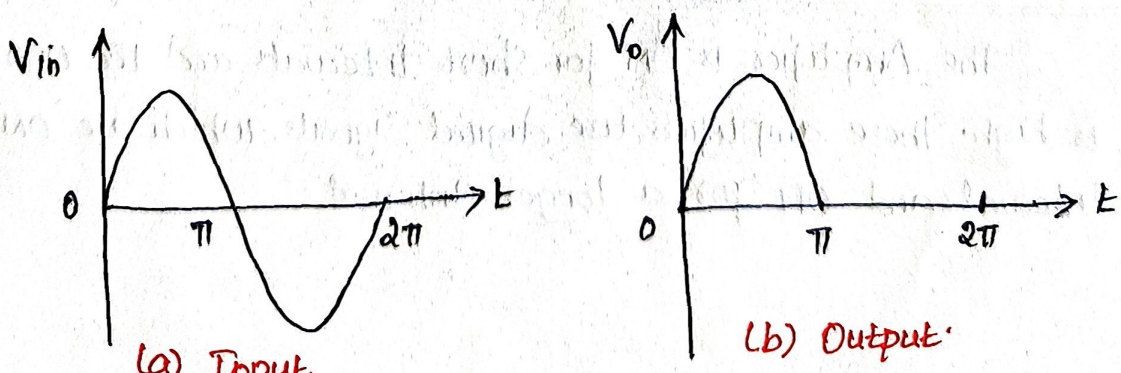


(a) Input (b) Output.

Fig. 1. Class A amplifier.

2. CLASS B AMPLIFIER

In class-B Amplifier, the Output signal is obtained only for one half Cycle of the Input signal. The thyristor conducts only in one half cycle of Input and. So, the Collector Current flows for only 180°.

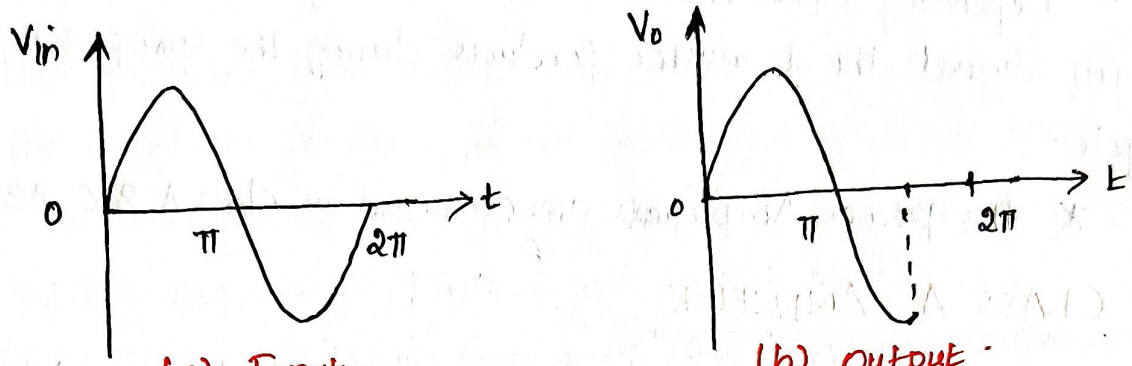


(a) Input (b) Output.

Fig. 2. Class B Amplifiers.

3. CLASS AB AMPLIFIERS

Class AB Amplifier has the characteristics in between class A and class B Amplifiers. The output current flows for more than half cycle but less than complete cycle. (i.e, more than 180° but less than 360°)

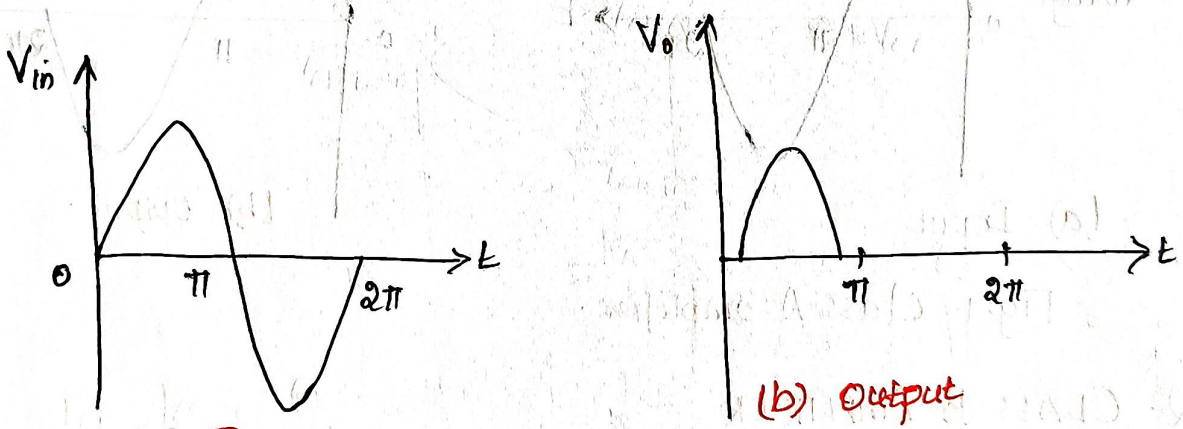


(a) Input (b) Output

Fig. 3. Class AB Amplifiers

4. CLASS C AMPLIFIERS

A power Amplifier is called as class C Amplifier if its output is obtained for less than half cycle period of its Input AC signal



(a) Input (b) Output

Fig. 4. Class C Amplifiers.

5. CLASS D AMPLIFIERS

The Amplifier is ON for short intervals and the overall Efficiency is high. These amplifiers use digital signals which are 'ON' for short interval and 'OFF' for a longer interval.

CLASS A AMPLIFIERS

The class A Amplifier is basically a Common Emitter Amplifier except that the Signals handled by power Amplifier circuit is in the range of Volts.

- The Transistor Bias and the Amplitude of the Input signal are such that the transistor Conducts for the entire cycle of Input signal.

* this is achieved by adjusting the Q-point at the Centre of the Load line so that maximum Output signal is obtained.

Fig.1 Shows the Basic Circuit of class A Amplifier. The operation of the Amplifier is restricted to smaller Central Region of the load line such that it can operate in the Linear Region of Load line

* Since the Transistor operates in the Linear Region of the Load line, the Output waveform is almost Similar to the Input waveform.

Fig.2 Shows the Ac load line and the Variation of I_C and V_{CE}

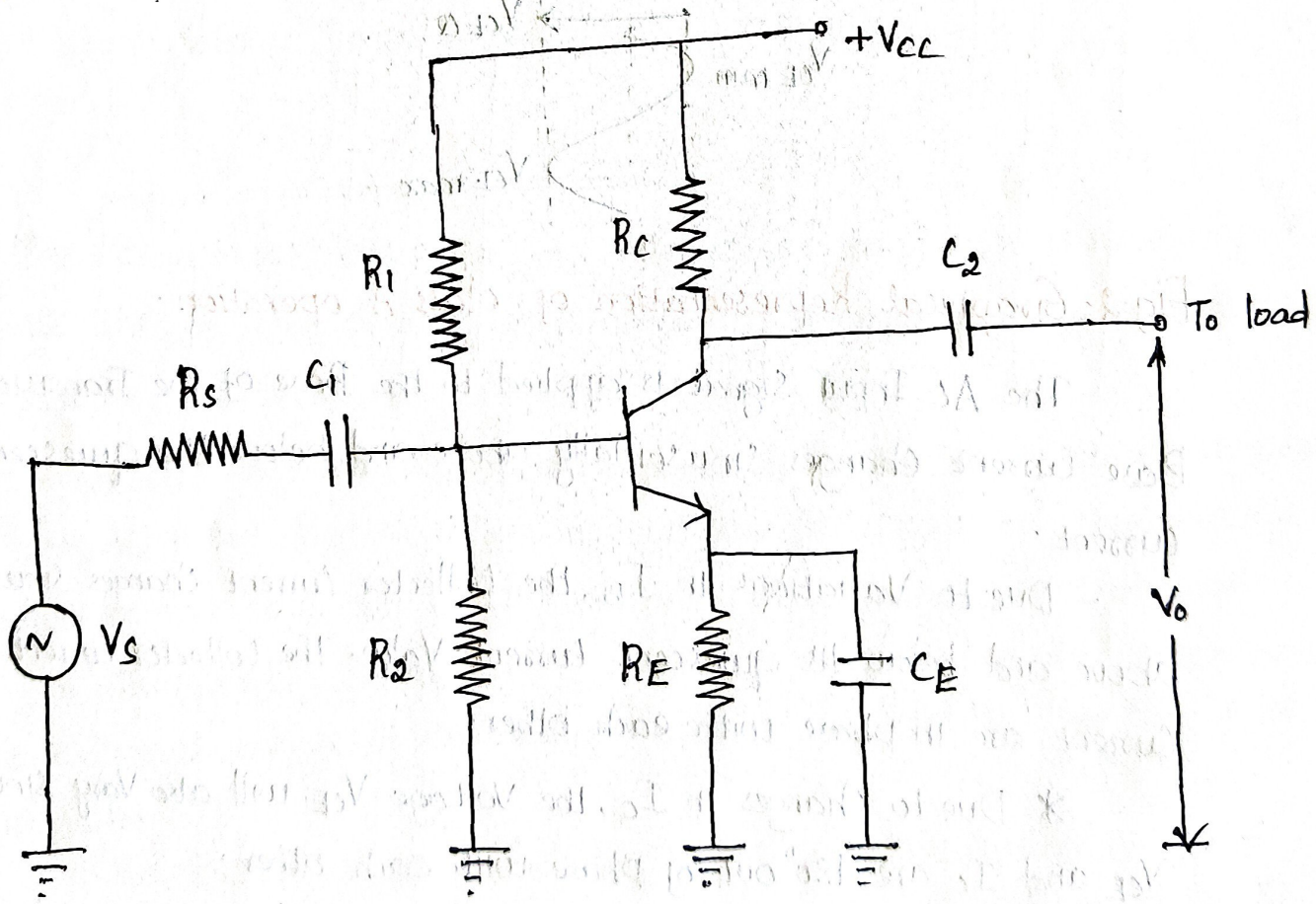


Fig.1. Class A Amplifier.

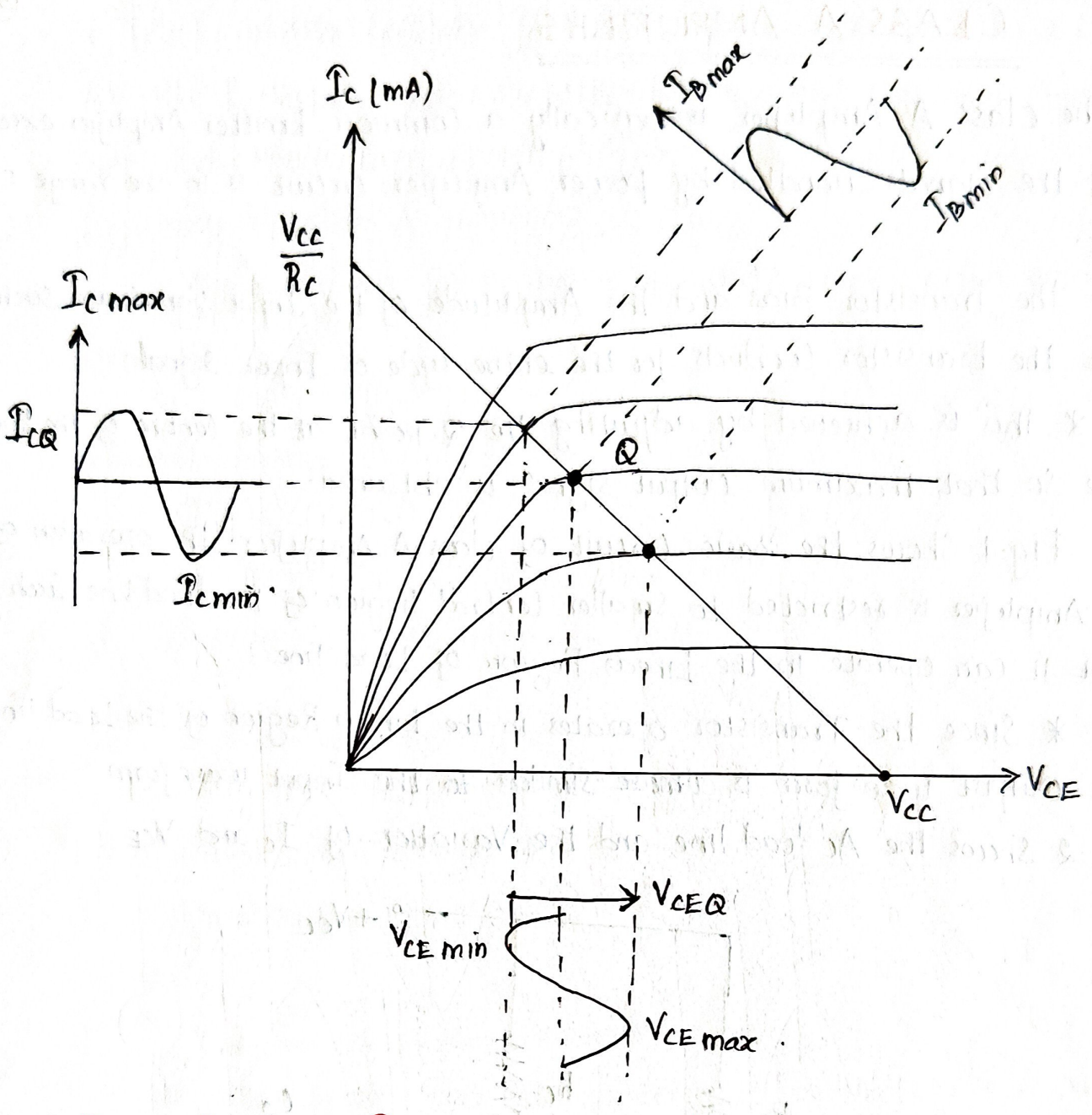


Fig.2. Graphical Representation of class A operation.

The AC Input Signal is applied to the Base of the Transistor and the Base Current changes sinusoidally above and below the quiescent Base Current.

- Due to Variations in I_B, the Collector Current changes sinusoidally above and below its quiescent Current Value. The Collector Current and Base Current are in phase with each other.

* Due to changes in I_C, the Voltage V_{CE} will also Vary sinusoidally. V_{CE} and I_C are 180° out of phase with each other.

- The transistor remains in the 'Active Region' for all the Values of Input Signal and Never enter into 'Saturation or Cut-off Regions'.

The transistor conducts for the complete cycle of ac Input (360°). So, V_{CE} and I_C across the transistor are high and the Input signal is amplified. Hence, large power will be dissipated in the transistor as heat. So, Efficiency of class A amplifiers is Low.

- Typical Value for Efficiency of Class A amplifier, lies between 25% and 50%.

ADVANTAGES :

1. Simple Construction.
2. No distortion in Output Voltage
3. Cheaper and less Bulky.

DISADVANTAGES :

1. Very Low Efficiency.
2. Large Power dissipation
3. High Output Impedance.

CLASS B AMPLIFIERS

The transistor conducts for only 180° or Half cycle of the Ac input Signal. The Q point of a class B amplifier is adjusted to be on the X-axis i.e, the transistor is biased at, cut-off.

- Hence, the transistor can conduct only during the positive Half cycle of the Ac Input Signal. When input signal is not applied, the transistor is Biased at cut-off and current will not flow through the Transistor

* The power dissipation is minimum in this condition. When the Input Signal is applied, an average amount of Current flows through the Transistor.

- Distortion is present at the output of the Transistor. To avoid distortion, two transistors are used instead of one Transistor. These two Transistors conduct in the alternate half cycles of the Input Signal so that the Input waveform is reproduced at the Output.

This can be done in two ways.

1. Class-B push pull Amplifier.
2. Class-B Complementary Symmetry Amplifier.

1. CLASS-B PUSH PULL AMPLIFIER

Fig.1 Shows the class-B push pull Amplifier. If the two transistors of same type (either PNP or NPN) are used then the Amplifier is called class-B push-pull Amplifier.

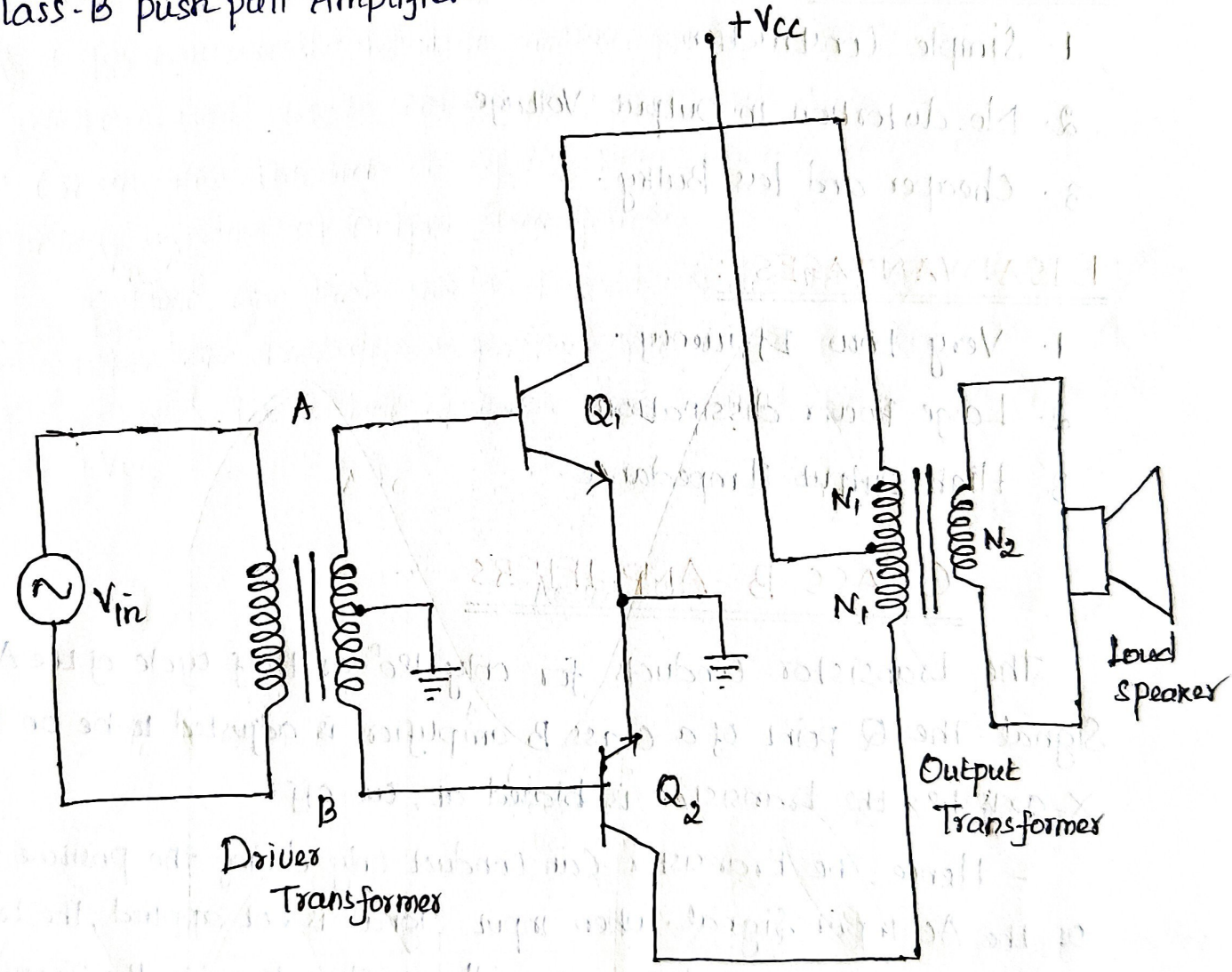


Fig.1. Class-B push pull Amplifier.

CONSTRUCTION :

The push-pull Amplifier uses two centre tapped Transformers. The Transformer on the Input side is known as 'driver Transformer' and the Transformer on the Load side is known as 'Output Transformer'

- The Input signal V_{in} is applied to the primary winding of the Input Transformer.

OPERATION :

When the Input signal is applied, the Emitter Base junction of 'Q_1' is forward biased during positive half of Input Signal. The Emitter-Base junction of Q_2 is Reverse biased.

– Thus Base Current flows for Q_1 and it is Zero for Q_2. So, the Collector current flows through upper half of the primary winding of the Output Transformer.

* During Negative half cycle of the input voltage, E-B junction of Q_1 is Reverse biased and E-B junction of Q_2 is forward biased i.e., Q_1 is OFF and Q_2 is ON.

– The Collector Current of Q_2 flows through Lower half of the Primary winding of Output Transformer.

* Here, one transistor is turned ON and the other is turned OFF i.e., when one transistor is pushed into conduction, the other conducting Transistor is pulled out of Conduction. So it is 'push-pull Amplifier'.

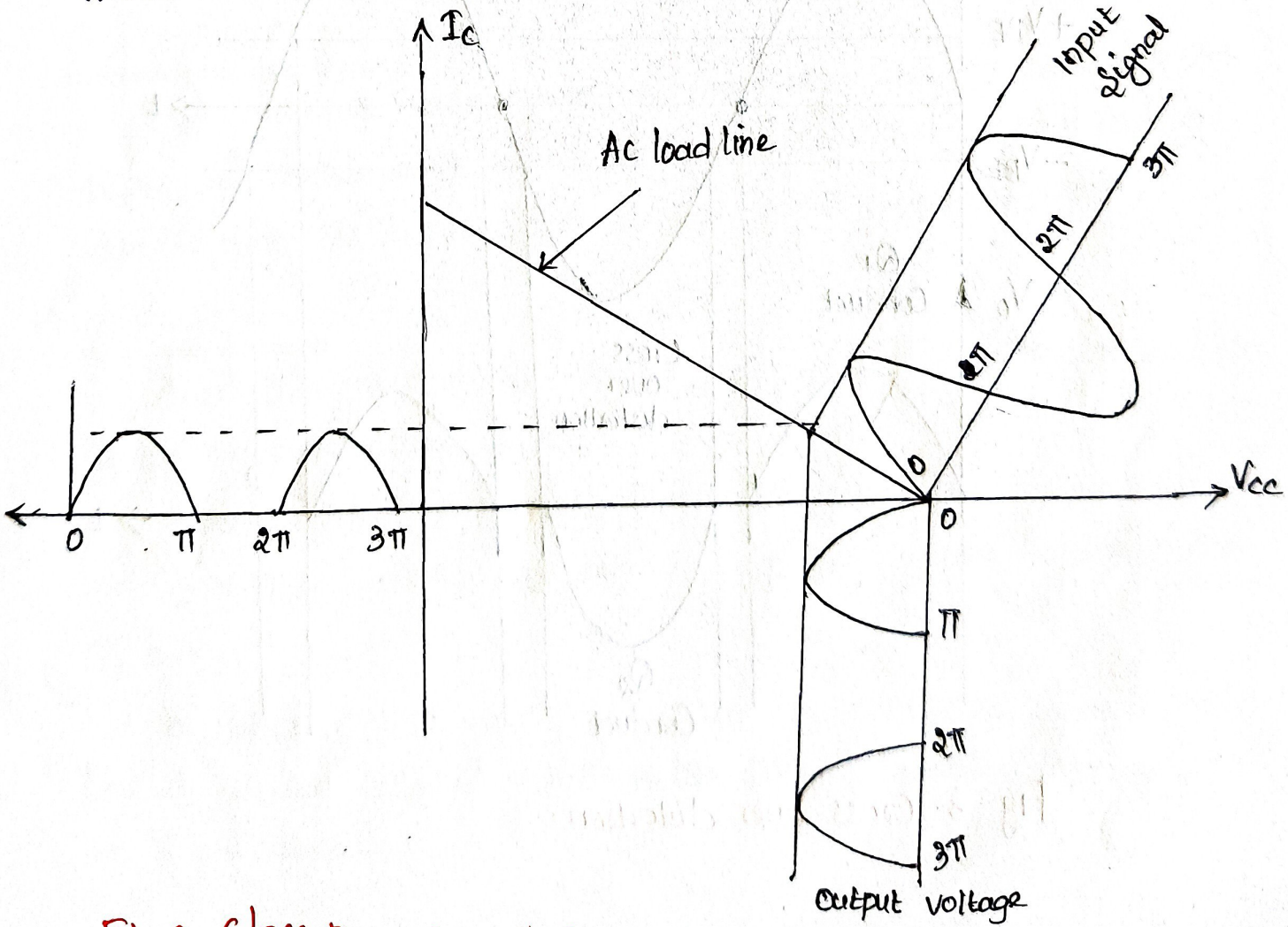


Fig.2. Class B push pull Amplifier operation.

CROSS OVER DISTORTION

This type of distortion occurs in class B amplifiers near the zero Crossing points.

- Class B amplifiers are biased at Cut-off Region when the Input Signal has greater voltage level than the barrier voltage, the Transistor conducts. Otherwise the Transistor will not conduct.

* During the time Interval between the conduction of the Transistors Q_1 and Q_2 at some point Neither of the transistors conduct. This results in a gap between the positive and Negative half of the Output signal and the output is not continuous signal. This distortion is called "Cross-over distortion"

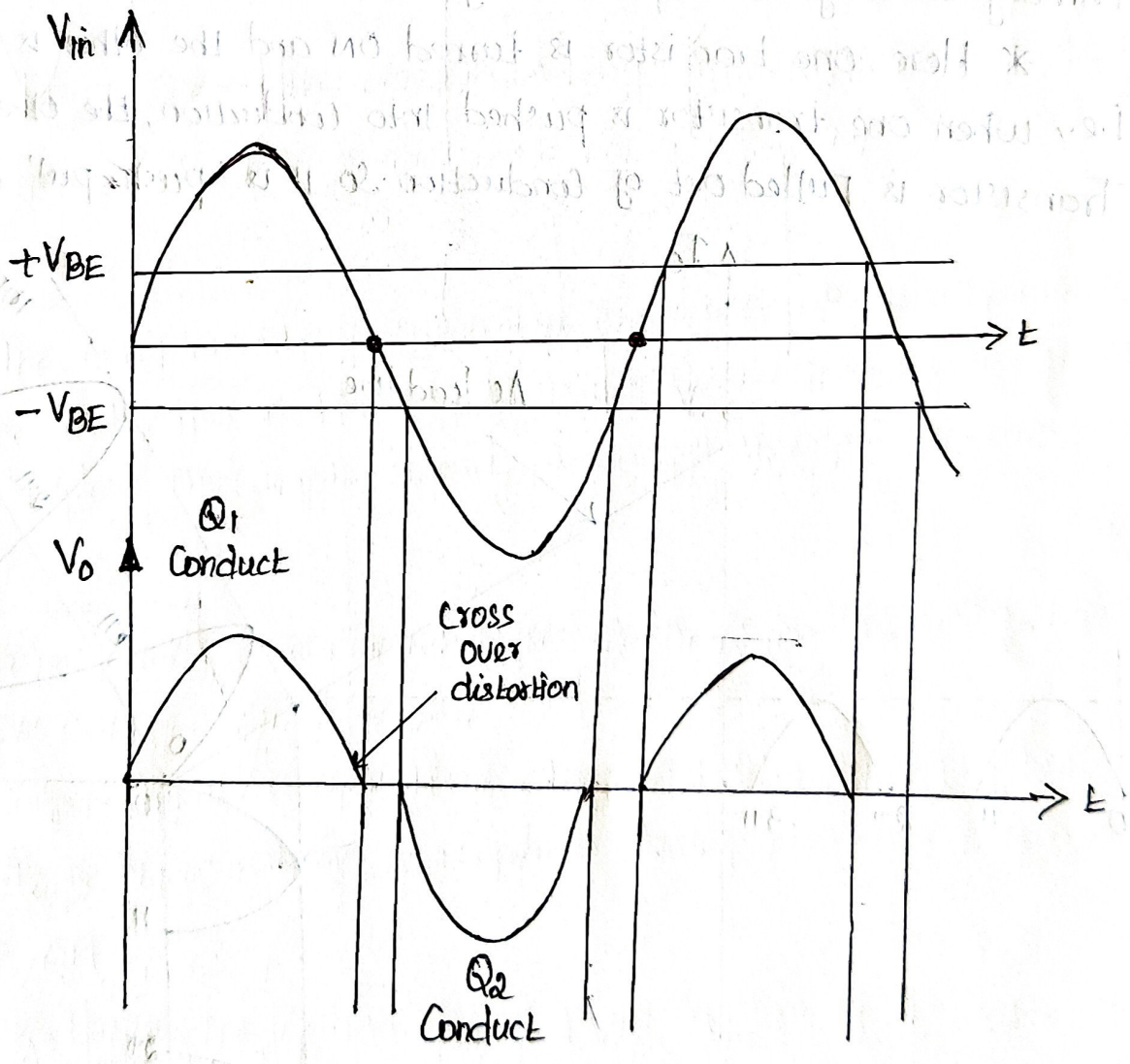


Fig. 3. Cross-over distortion.

ADVANTAGES OF CLASS-B PUSH PULL AMPLIFIERS

1. The Efficiency of class-B Amplifier is 78.5 % which is very much greater than class-A (25 %)
2. Zero power dissipation under quiescent conditions.
3. Even order Harmonics are cancelled
4. Impedance Matching is possible.

DISADVANTAGES :

1. Cross over distortion is Present
2. Supply Current changes with the signal

2. COMPLEMENTARY SYMMETRY CLASS-B AMPLIFIER

Fig. 1 shows the Complementary Symmetry push-pull class-B Amplifier. Here, transformers are not used.

CONSTRUCTION :

The Complementary Symmetry Amplifiers uses two transistors one is NPN and other is PNP. Symmetry indicates that biasing Resistors are Equal. The Input Signal is coupled through Capacitor.

OPERATION :

When there is no Input signal, both Q_1 and Q_2 will not conduct. So, the Output Voltage is zero.

- When Input is applied, Q_1 conducts during positive half cycle and Q_2 is OFF. Similarly, Q_2 conducts during Negative half cycle and Q_1 is OFF

* Hence, the Output Signal is the replica of the Input signal. Due to Emitter follower operation, the Output Signal is in phase with the Input Signal.

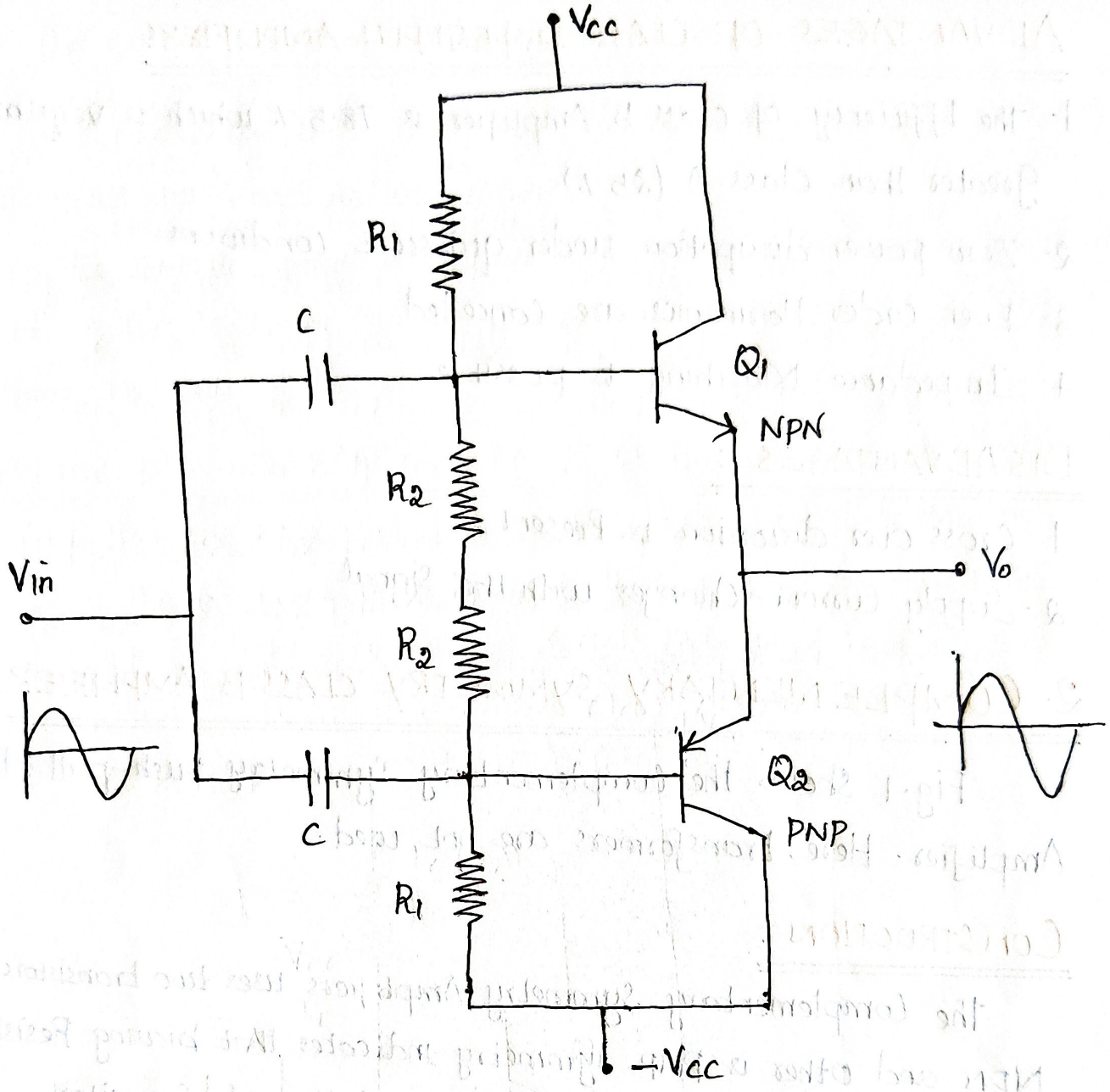


Fig. 1. Class-B Complementary Symmetry Amplifier.

ADVANTAGES :

1. Transformers are not used. So, the Amplifiers are less Expensive and less Bulky.
2. Efficiency is greater than Class-B push pull Amplifiers
3. Impedance Matching is possible.

DISADVANTAGES :

1. A dual polarity Supply (+Vcc, -Vcc) is required
2. Cross over distortion is present in Output.

CLASS AB AMPLIFIERS

To overcome the cross over distortion in class B amplifiers, we are going for 'class AB Amplifiers'.

- The output signal is obtained for more than 180° but less than 360° of the AC Input signal. The Q point is adjusted to be slightly above the Cut-off Region.

CONSTRUCTION AND OPERATION :

Fig.1 show the circuit diagram of class AB push pull Amplifiers. The class B push pull Amplifier is converted to class AB push pull Amplifier by connecting a Resistor R and Diode D in the circuit.

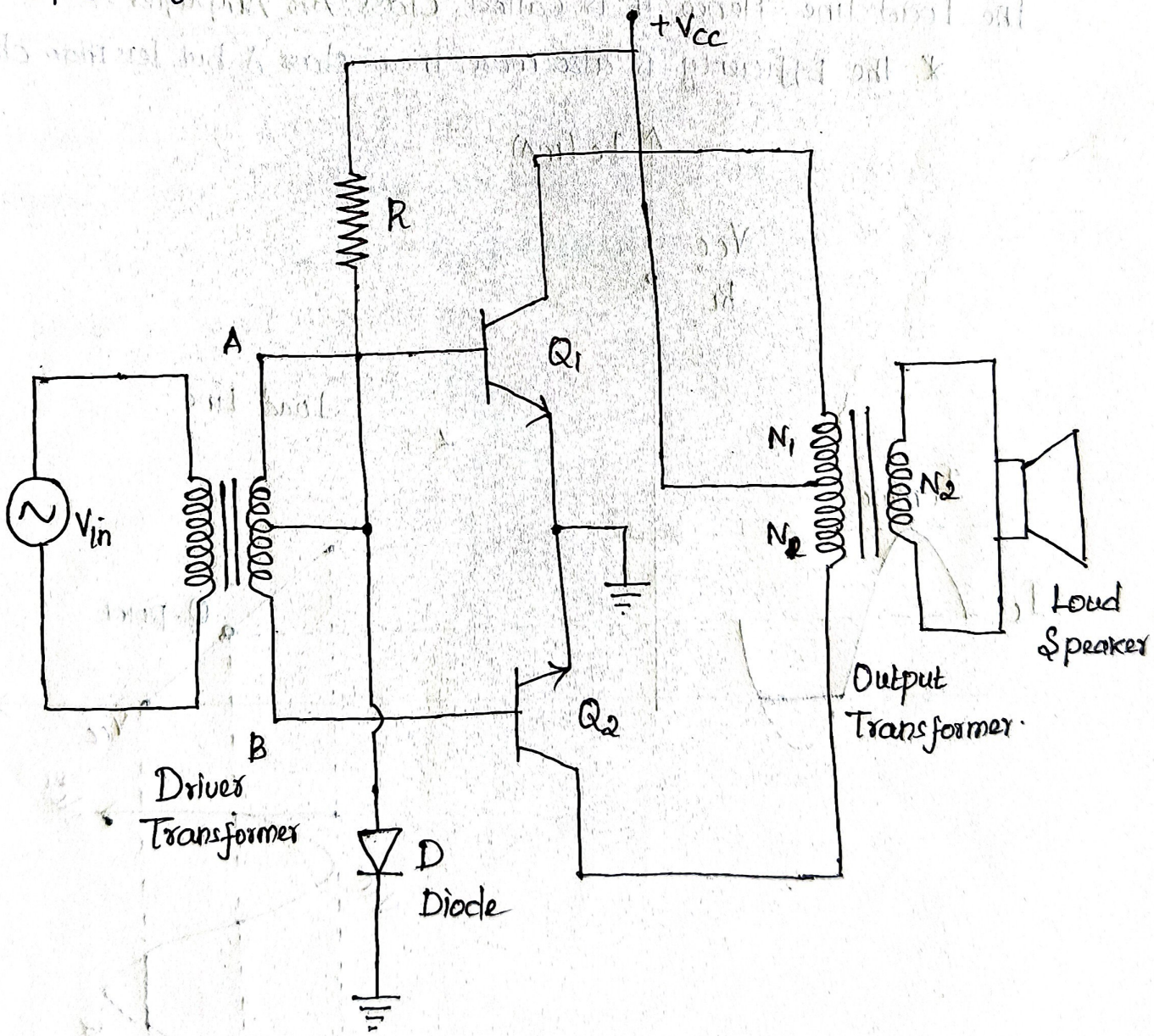


Fig.1. Class AB push pull Amplifier

The Output of the diode is connected to bases of both transistors through the Secondary winding of Input Transformer. This provides the required dc bias for the Transistors.

- Here, the transistors will conduct for complete half cycle of the Input Signal and the Cross-over distortion will be avoided.

* the Q-point is slightly shifted above the X-axis. The transistor Q_1 conducts during entire positive half cycle and Q_2 conducts during entire Negative half cycle of Input. This is achieved due to the fact that the bias provided by the diode is equal to the cut-in voltage.

- The Q-point is in between that for class A and class B i.e., Q-point is slightly above the X-axis but below the mid-point of the Load line. Hence it is called 'Class AB Amplifier'

* The Efficiency is also more than class 'A' but less than class 'B'

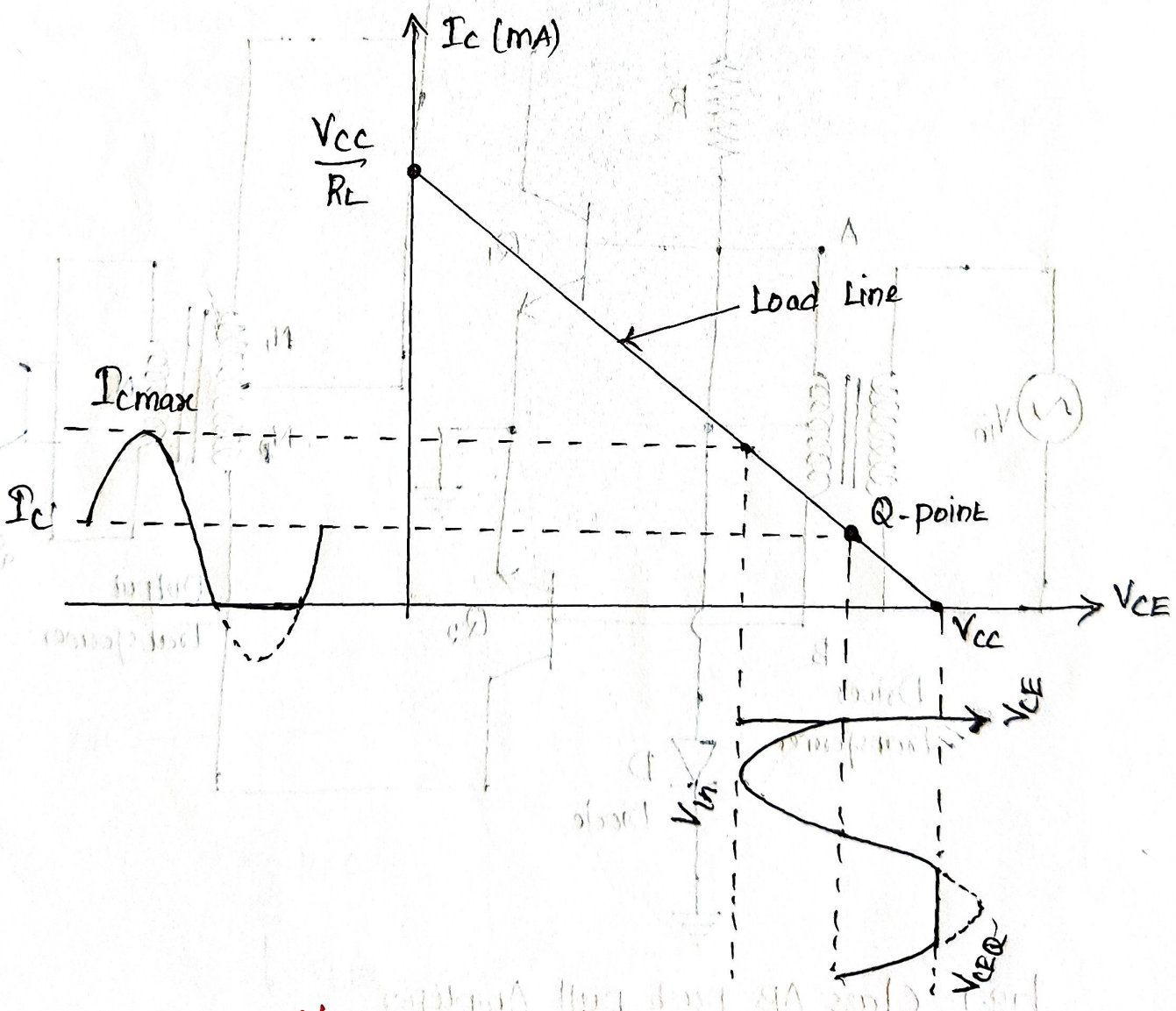


Fig. 2. Class AB operation.

ADVANTAGE :

1. Cross over distortion is eliminated.

CLASS C AMPLIFIERS

In class C Amplifiers, the output signal is obtained for less than a half cycle period of the Input AC signal. The operating point is adjusted to be below the X-axis i.e., the transistor is biased below Cut-off Region.

- Class C Amplifiers cannot be used as 'Audio Amplifiers'. They are mainly used as Tuned Circuits in Communication Systems.

CONSTRUCTION :

Fig.1 shows the circuit diagram for class C Amplifier. The LC Tuned Circuit is used as the Load for the transistor Q. The Negative Base Voltage biases the transistor below cut-off Region

- The Input Voltage Vin is applied to the Base of Transistor. This Voltage is Super Imposed on $-V_{BB}$.

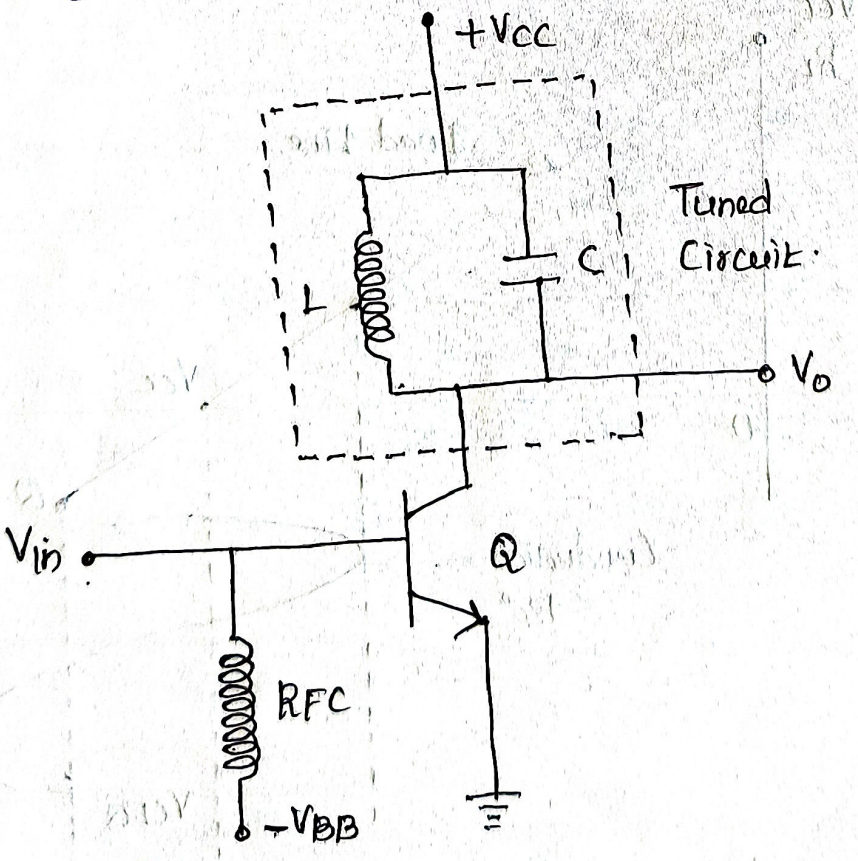


Fig.1. Class C Amplifier.

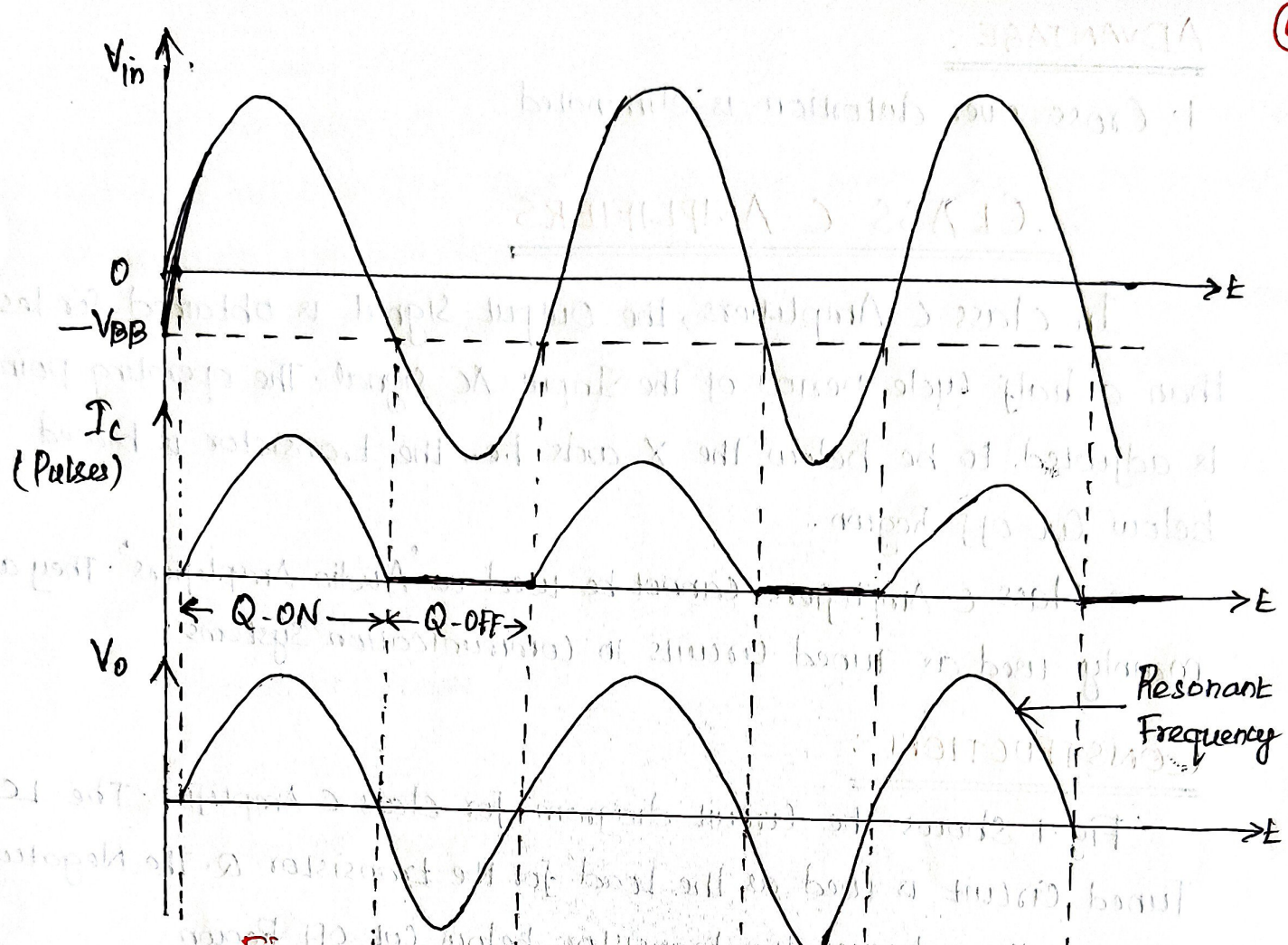


Fig. 2. Class C operation

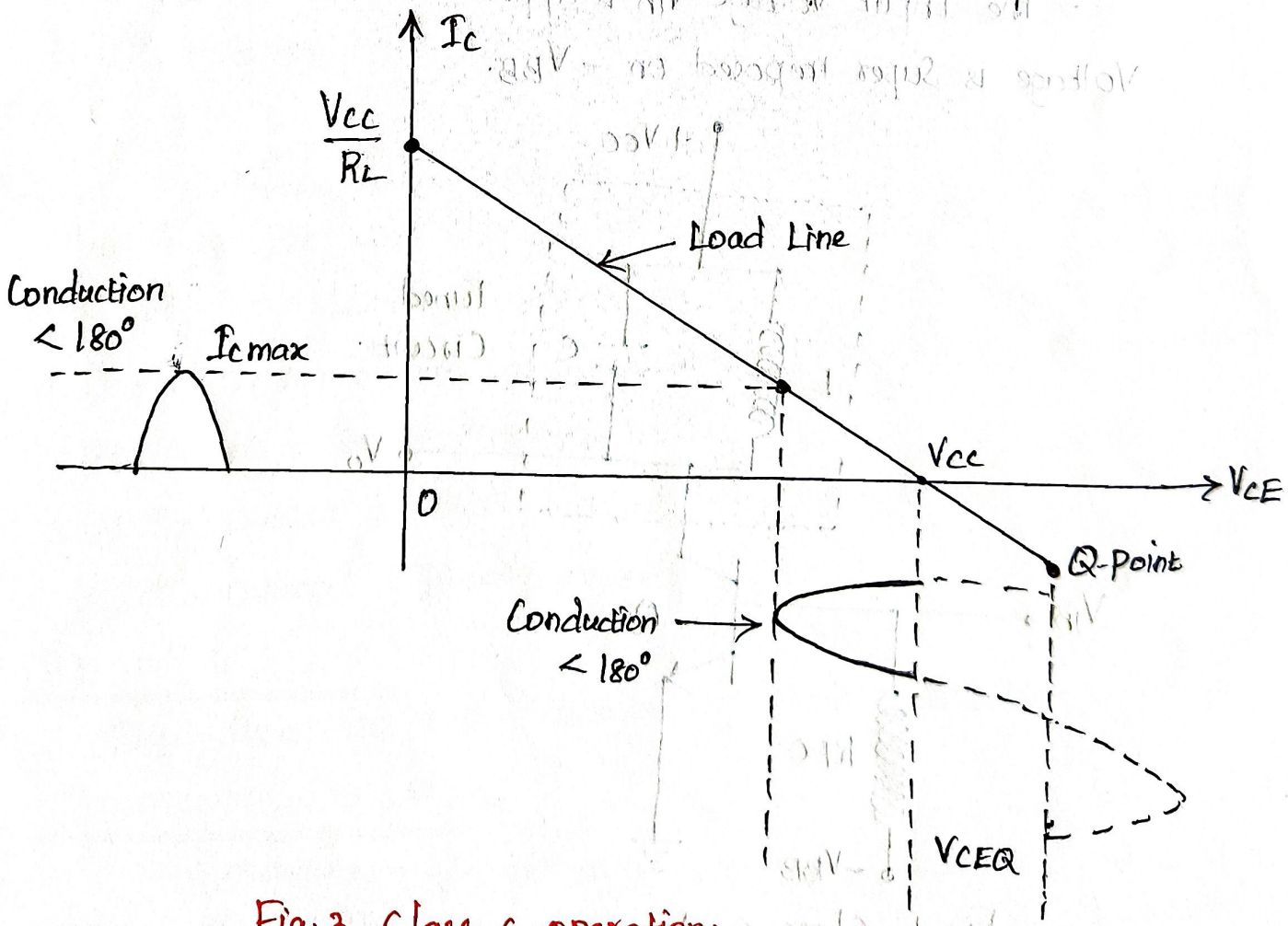


Fig. 3 Class C operation.

OPERATION

The transistor Q is forward biased and will conduct for an angle which is less than 180°. Thus the collector current flows in the form of pulses with duration less than 180°.

– These current pulses are applied to the LC Resonant circuit and the output signal is obtained at the Resonant Frequency of the tuned circuit. Thus class C Amplifier is used at the Resonant Frequency only.

ADVANTAGES :

1. Very High Efficiency (>98 %)
2. Minimum Power Lost

DISADVANTAGES

1. Distortion may occur.

APPLICATIONS :

1. Tuned Amplifiers
2. As collector Modulator to Produce AM (Amplitude Modulated) signal

CLASS D AMPLIFIERS

This Amplifier uses digital signals which are ON for short Interval and OFF for a Longer Interval.

i) Any Input signal can be converted to digital or pulsed waveform before giving it to the Amplifier.

ii) The output is obtained from many pieces of the Input signal

iii) the overall Efficiency is Very High.

BLOCK DIAGRAM :

Fig.1 shows the Block diagram of class D Amplifier.

1. SAWTOOTH GENERATOR :

It generates a high Frequency Saw tooth waveform and it is applied at the Inverting Terminals.

The Sawtooth waveforms have frequency greater than that of input Signal.

2. COMPARATOR :

This comparator compares the sine wave input and the Sawtooth waveform. Its output is a pulse width modulated waveform.

3. Amplifier :

The pulse signal is amplified by the Amplifier without modifying the shape of the pulses. The transistor acts as a switch which is in either ON or OFF condition.

- When the transistor is ON, the output current is produced.

4. LOW PASS FILTER :

It converts the Amplified pulse waveform into sinusoidal signal i.e., the output is the amplified form of the Input signal

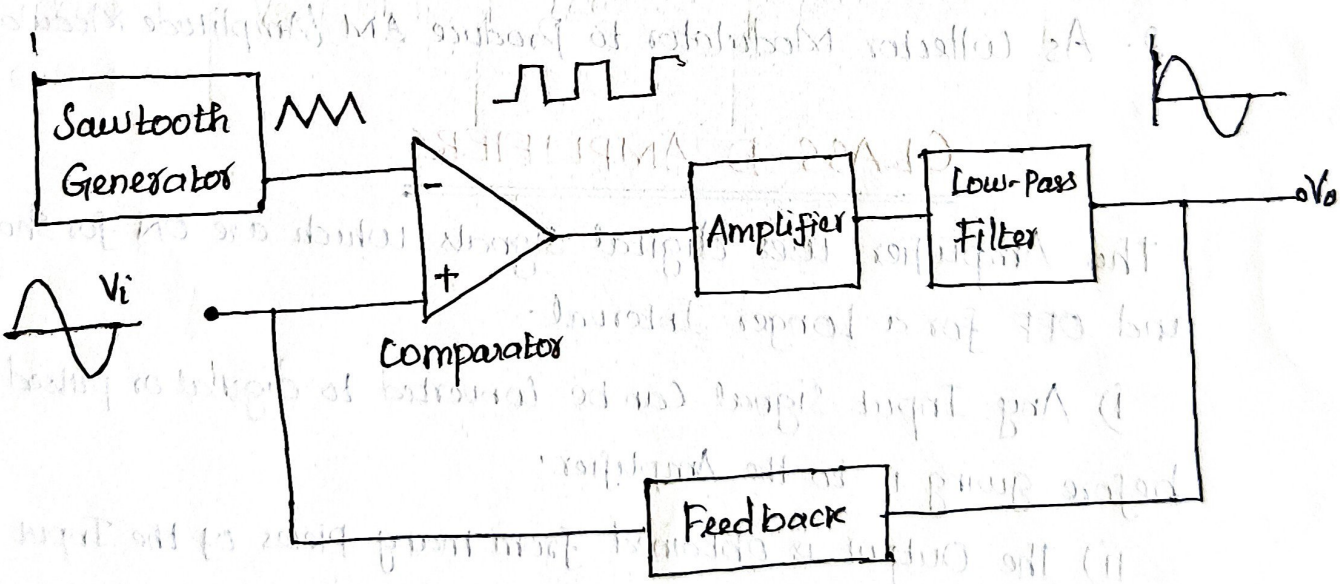
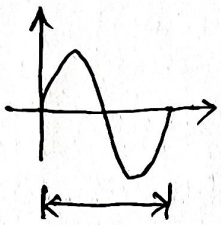
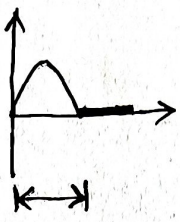
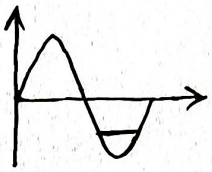
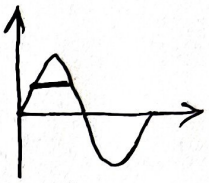


Fig. 1. Class D Amplifier

ADVANTAGES :

1. High Efficiency (>90%)
2. Both Analog and digital signals can be Amplified.

Comparision of different Types of Power Amplifier.

S. No.	Parameter	Class A	Class B	Class AB	Class C
1.	Conduction Angle	360° 	180° 	Between 180° and 360° 	less than 180° 
2.	Q-point	Center	On X-axis	Above X-axis and Below the mid point	Below X-axis
3.	Distortion	No distortion	Cross-over distortion	Low	More than A, B and AB
4.	Efficiency	25-50 %	78.5 %	50-78.5 %	95 %
	Power dissipation	Very High	Low	Moderate	Very Low.

UNIT - V

FEEDBACK AMPLIFIERS AND OSCILLATORS

INTRODUCTION

An Ideal Amplifier will provide a stable output which is an amplified version of the Input signal

– But the Gain and Stability of practical Amplifiers is not very Good. because of device parameter variation or due to changes in Ambient Temperature and Non-linearity of the device.

* The feedback can be either Negative (degenerative) or Positive (Regenerative)

i) In Negative Feedback, a portion of the output signal is Subtracted from the Input signal to produce desired output.

ii) In positive Feedback, a portion of the output signal is added to the Input signal to produce desired output

* Negative Feedback plays an Important role in almost all the amplifier stabilization of biasing circuits, it causes the Location of the quiescent point (Q) to become stable.

– Thus it maintains a constant Value of Amplifier Gain against Temperature Variation Supply Voltages etc,

ADVANTAGES OF NEGATIVE FEEDBACK

1. Higher Input and Lower output Impedance.
2. Improved Gain Sensitivity.
3. Reduced Noise
4. Increased Bandwidth
5. Reduced Distortion.

DISADVANTAGES

1. Reduced Circuit overall Gain
2. Reduced Stability at High Frequency

INPUT AND OUTPUT RESISTANCE WITH FEEDBACK

There are four basic ways of Connecting the Feedback signal. Both Current or Voltage can be fedback to the Input either in Series or parallel, accordingly it can be classified as

1. Voltage Series Feedback Connection
2. Current Series Feedback Connection
3. Voltage Shunt Feedback Connection
4. Current Shunt Feedback Connection.

The first term (represents the Parameter taken as Feedback Value). 'Voltage' refers to Connecting Output Voltage as input to the Feedback Network.

- Similarly the term 'Current' refers to taking off Output Current as the Input to Feedback Network.

* The Second term (represents the way in which it is applied with Input) 'Series' refers to Connecting the feedback signal in Series to the Input signal, and term 'Shunt' refers to Connecting the feedback signal in shunt with an Input Source.

1. VOLTAGE SERIES FEEDBACK :

In this the Output Voltage is directly Proportional to the Input Voltage, thus it is used as 'Voltage Amplifier'

$$A = \frac{V_o}{V_i} \quad (or) \quad \boxed{V_o = A V_i}$$

2. VOLTAGE SHUNT FEEDBACK

In this the Output Voltage is directly proportional to Input Current. It is used as 'Transresistance Amplifier'

$$A = \frac{V_o}{I_i} \quad (or) \quad \boxed{V_o = A I_i}$$

3. CURRENT SERIES FEEDBACK

In this the Output Current is directly proportional to the Input Voltage, hence it is used as 'TransConductance Amplifier'.

$$A = \frac{I_o}{V_i} \quad (or) \quad \boxed{I_o = A V_i}$$

4. CURRENT SHUNT FEEDBACK

It means that the Output Current is directly Proportional to the Input Current. It is used as 'Current Amplifier'.

$$A = \frac{I_o}{I_i} \quad (or) \quad \boxed{I_o = A I_i}$$

VOLTAGE SERIES FEEDBACK

Fig. 1 shows the block diagram of Voltage Series Feedback. A Sample of Output Voltage i.e., $\boxed{V_f = \beta V_o}$ is connected in Series opposition to the Input Voltage Signal V_s

* The Gain of the Amplifier with Feedback is as follows:

$$\boxed{A_f = \frac{V_o}{V_i}}$$

A_i - Gain of the Amplifier without Feedback.

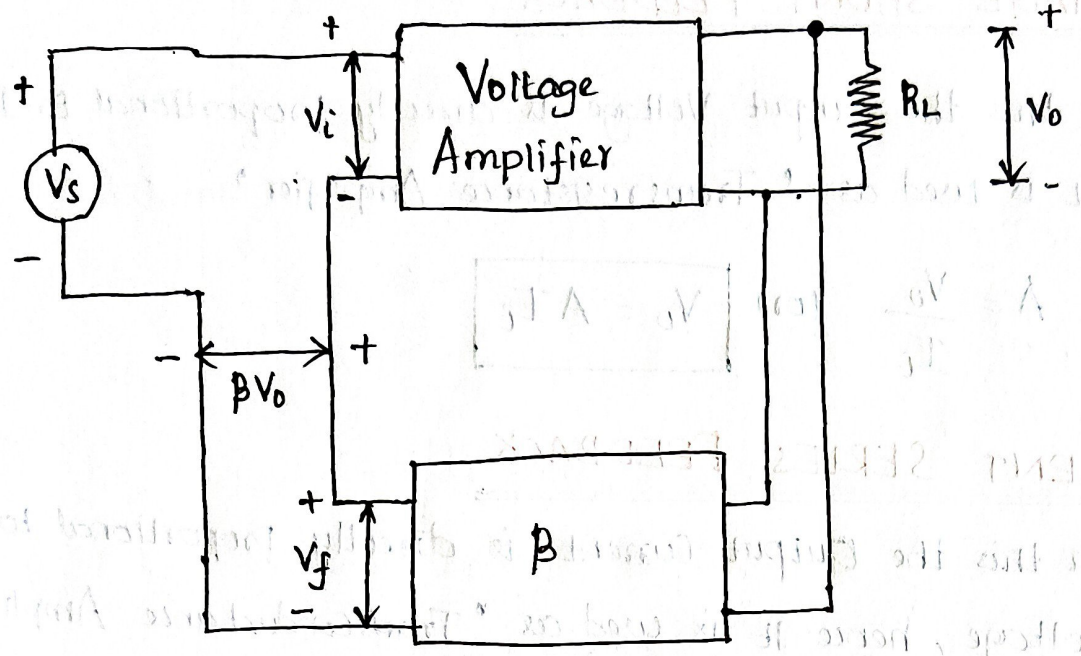


Fig.1 Voltage Series Feedback

If Feedback is Connected then

$$V_S = V_i + V_f \quad (or)$$

$$V_i = V_S - V_f$$

$$V_S = V_i + \beta V_o$$

$$= V_i + \beta A V_i$$

$$V_S = V_i (1 + \beta A)$$

$$A_{VF} = \frac{V_o}{V_S} = \frac{V_i A}{(1 \pm A\beta) V_i}$$

$$\boxed{A_{VF} = \frac{A}{1 + A\beta}}$$

i) Input Impedance (Z_{IF})

The equivalent Circuit for Voltage Series Feedback Connection is Shown in fig.2.

- In this Case the Basic Amplifier is modeled as the Voltage dependent Voltage Source. Its Input Impedance is determined below.

$$V_i = V_s - V_f.$$

We Know ; $V_i = R_i I_i$

Assuming R_o to be Negligible

$$V_s = V_i + V_f$$

$$= R_i I_i + \beta V_o$$

$$= R_i I_i + \beta A V_i$$

$$= R_i I_i + \beta A R_i I_i$$

$$V_s = I_i R_i [1 + A\beta]$$

$$Z_{if} = \frac{V_s}{I_i} = \frac{I_i R_i [1+A\beta]}{I_i} \qquad [R_i = Z_i]$$

$$\boxed{Z_{if} = Z_i (1+\beta)}$$

ii) OUTPUT IMPEDANCE (Z_{OF})

From fig.

$$V_o = IZ_o + AV_i$$

$$V_o = IZ_o - AV_f$$

Assume $R_o = Z_o$

(as we know $V_i = V_s - V_f$. V_s is transferred to the output side to find the Output Impedance hence $V_s = 0$, thus $V_i = -V_f$)

$$V_o = IZ_o - A\beta V_o \qquad [V_f = \beta V_o]$$

$$V_o + A\beta V_o = IZ_o$$

$$V_o (1+A\beta) = IZ_o$$

$$V_o = \frac{IZ_o}{1+A\beta}.$$

$$Z_{OF} = \frac{V_o}{I_o} = \frac{I Z_o}{(1+A\beta) I_o}$$

$$\boxed{Z_{OF} = \frac{Z_o}{1+A\beta}}$$

Z_{OF} - Output Impedance of the Amplifier with Feedback

Z_o - Output Impedance of the Amplifier without Feedback.

Thus the output impedance is reduced by a factor of $(1+A\beta)$ from the Output Impedance of the Amplifier without Feedback.

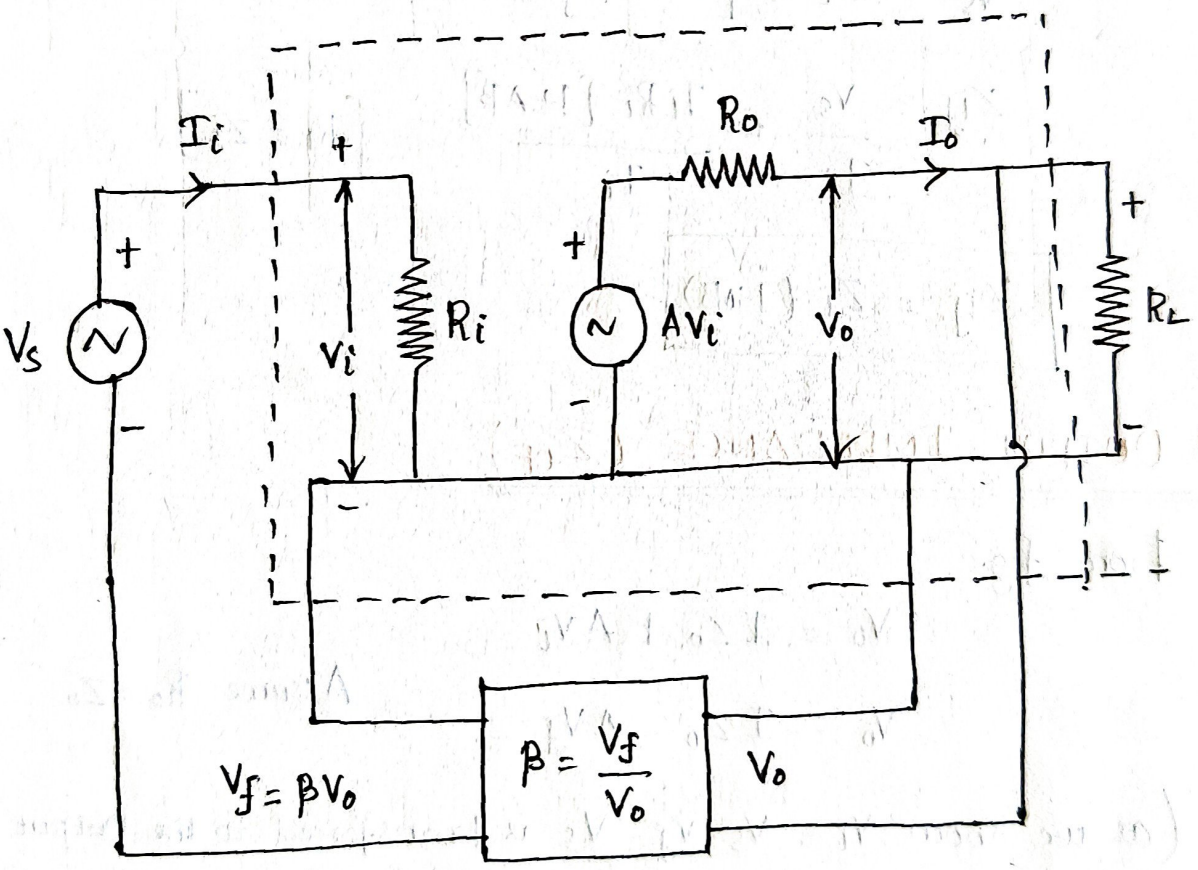


Fig. 2. Equivalent Circuit.

VOLTAGE SHUNT FEEDBACK

Fig.3 shows the block diagram for Voltage Shunt Feedback Connection. In this case the Output Voltage is fed in Parallel with the Input circuit, thus it is called as 'Voltage Shunt Feedback'.

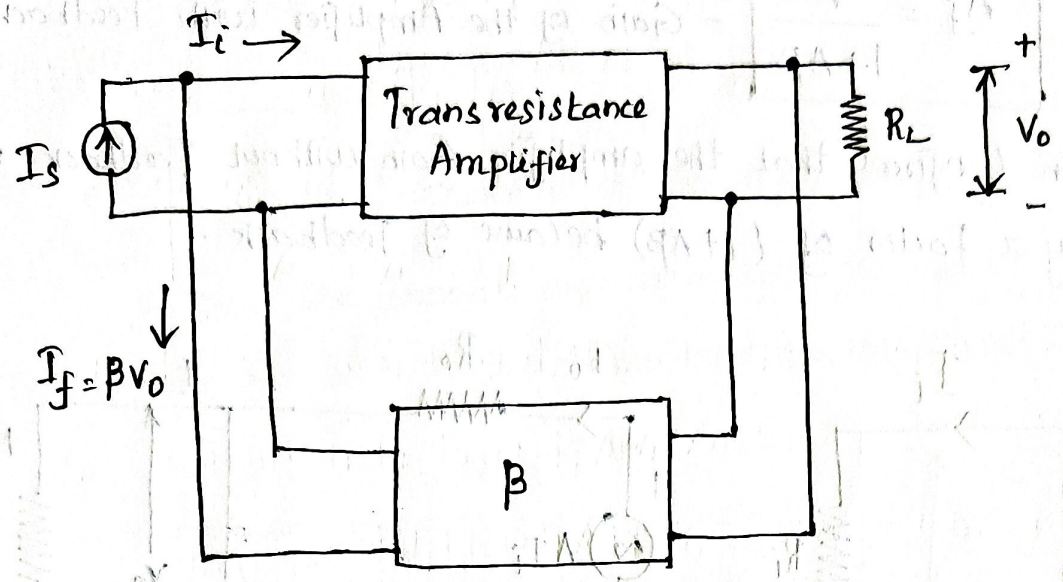


Fig.3 Voltage Shunt Feedback

The Output is V_o and because of Feedback is Connected in Parallel, the potential difference across all the elements are Same, ~~but~~ — But Current will Vary thus the Input parameter (Because of Shunt Connection) is I_i, the Ratio of V_o/I_i is known as 'Transresistance' thus Configuration acts as Transresistance Amplifier.

$$A = \frac{V_o}{V_i} = \text{Gain of Amplifier without Feedback}$$

$$\beta = \frac{I_f}{V_o}$$

$$I_s = I_i + I_f$$

$$= I_i + \beta V_o$$

$$= I_i + \beta A I_i$$

$$\boxed{I_s = I_i (1 + A\beta)}$$

$A = V_o/V_i$

$V_i = V_o = A V_i$

$$A_f = \frac{V_o}{I_s}$$

$$= \frac{V_o}{I_i (1+A\beta)} = \frac{A I_i}{I_i (1+A\beta)} = \frac{A}{1+A\beta}$$

$$A_f = \frac{A}{1+A\beta}$$ = Gain of the Amplifier with Feedback.

This again confirms that the amplifier Gain without Feedback is reduced by a Factor of $(1+A\beta)$ because of Feedback.

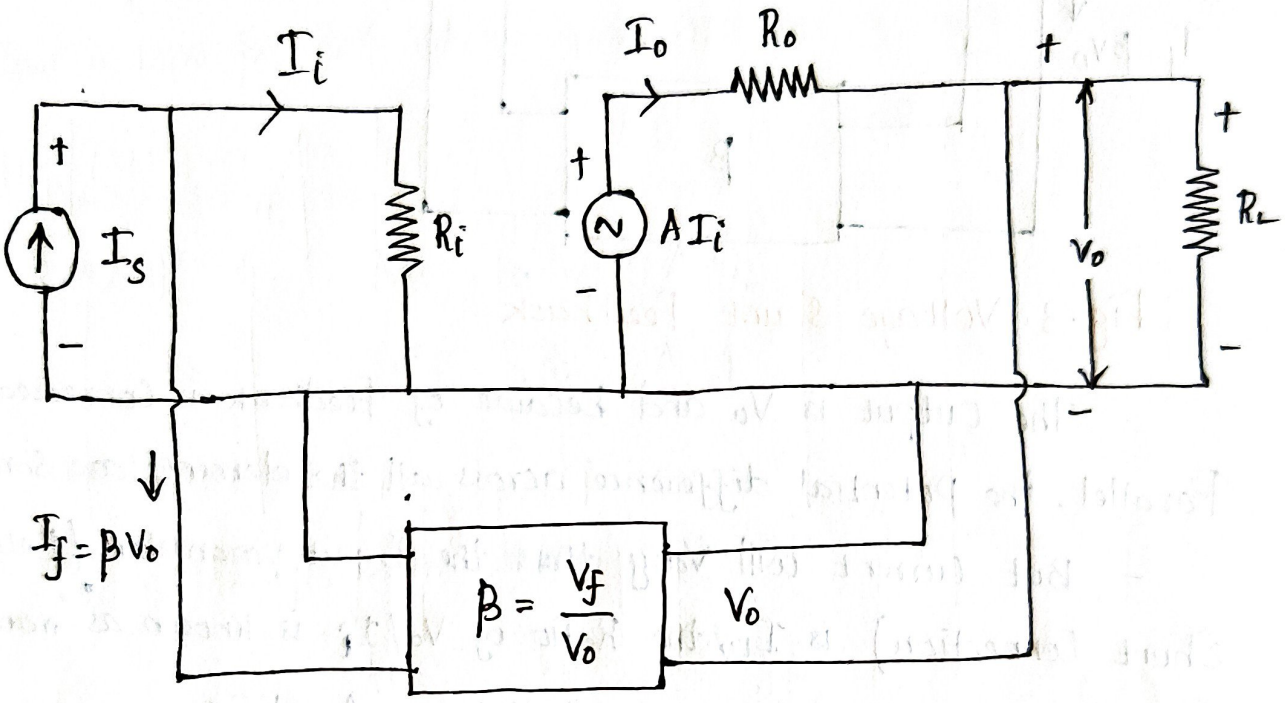


Fig. 4. Equivalent Circuit of Voltage Shunt Feedback

i) Input Impedance (Z_{if})

A Voltage Shunt Feedback connection with Basic Amplifier modified as Current dependent Voltage Source is as shown in fig. 4.

The Input Impedance with Feedback is given by

$$Z_{if} = \frac{V_i}{I_s} = \frac{V_i}{I_i + I_f}$$

$\therefore I_f = \beta V_o$

$V_o = AI_i$

$V_o = AI_i$

$$= \frac{V_i}{I_i + \beta V_o} = \frac{V_i}{I_i + \beta A I_i}$$

$$= \frac{V_i}{I_i (1+A\beta)}$$

$$Z_{if} = \frac{Z_i}{1+A\beta}$$

$Z_i = \frac{V_i}{I_i}$ = Input Impedance of Amplifier without Feedback.

* Thus the Input Impedance gets reduced by a Factor $(1+A\beta)$.

This is true for both Voltage Shunt and Current Shunt Feedback Connections.

ii) OUTPUT IMPEDANCE : (Z_{OF})

From fig. 4, $V_o = I_o R_o + A I_i$

$= I_o R_o - A I_f$

We know, $I_i = I_s - I_f$

I_s is transferred to output side, thus $I_s = 0$,

$I_i = -I_f = -\beta V_o$

$\therefore V_o = I_o R_o - A I_f$ $\quad I_f = \beta V_o$

$V_o = I_o R_o - A\beta V_o$

$V_o + A\beta V_o = I_o R_o$

$V_o(1+A\beta) = I_o R_o$

$$V_o = \frac{I_o R_o}{(1+A\beta)}$$

$$R_{OF} = \frac{V_o}{I_o}$$

$$= \frac{I_o R_o}{I_o(1+A\beta)}$$

$$R_{OF} = \frac{R_o}{1+A\beta}$$

Thus the equation shows that Output Impedance of Voltage Shunt Feedback is also reduced by the desensitivity factor of $(1+A\beta)$ from the Output Impedance of Amplifier without Feedback $Z_o = R_o$.

CURRENT SERIES FEEDBACK

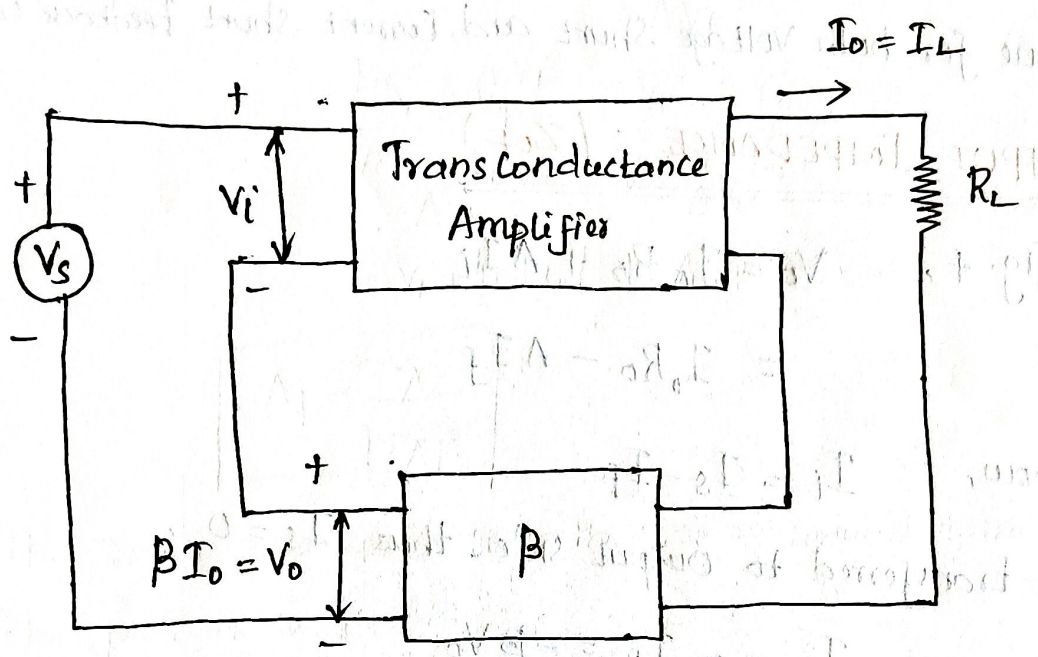


Fig.5. Current Series Feedback

Above fig.5 shows the block diagram of Current Series Feedback. In this Configuration, the Output Current is taken as Feedback Value and is Connected in Series with Input Circuits

- Thus the Input parameters is V_i i.e., Input Voltage is Proportional to Output Current. The Ratio of I_o/V_i is known as term Conductance thus this Configuration is Called as 'Trans Conductance Amplifier'

* The Property of Trans Conductance Amplifier is $R_i >> R_s$ and $R_o >> R_L$ thus $I_o = I_L$

$$A = \frac{V_o}{V_i} = \text{Gain of the Amplifier without feedback.}$$

$$\beta = \frac{V_f}{I_o} = \text{Feedback Factor.}$$

$$V_s = V_i + V_f$$

The Gain of the Amplifier with Feedback is given by

$$A_f = \frac{I_o}{V_s}$$

$$= \frac{I_o}{V_i + V_f} = \frac{AV_i}{V_i + \beta I_o}$$

$$I_o = AV_i$$

$$= \frac{AV_i}{V_i + \beta A V_i} = \frac{AV_i}{V_i(1+A\beta)}$$

$$\boxed{A_f = \frac{A}{1+A\beta}}$$

This result also shows that the gain is reduced by the factor $(1+A\beta)$ when feedback is provided.

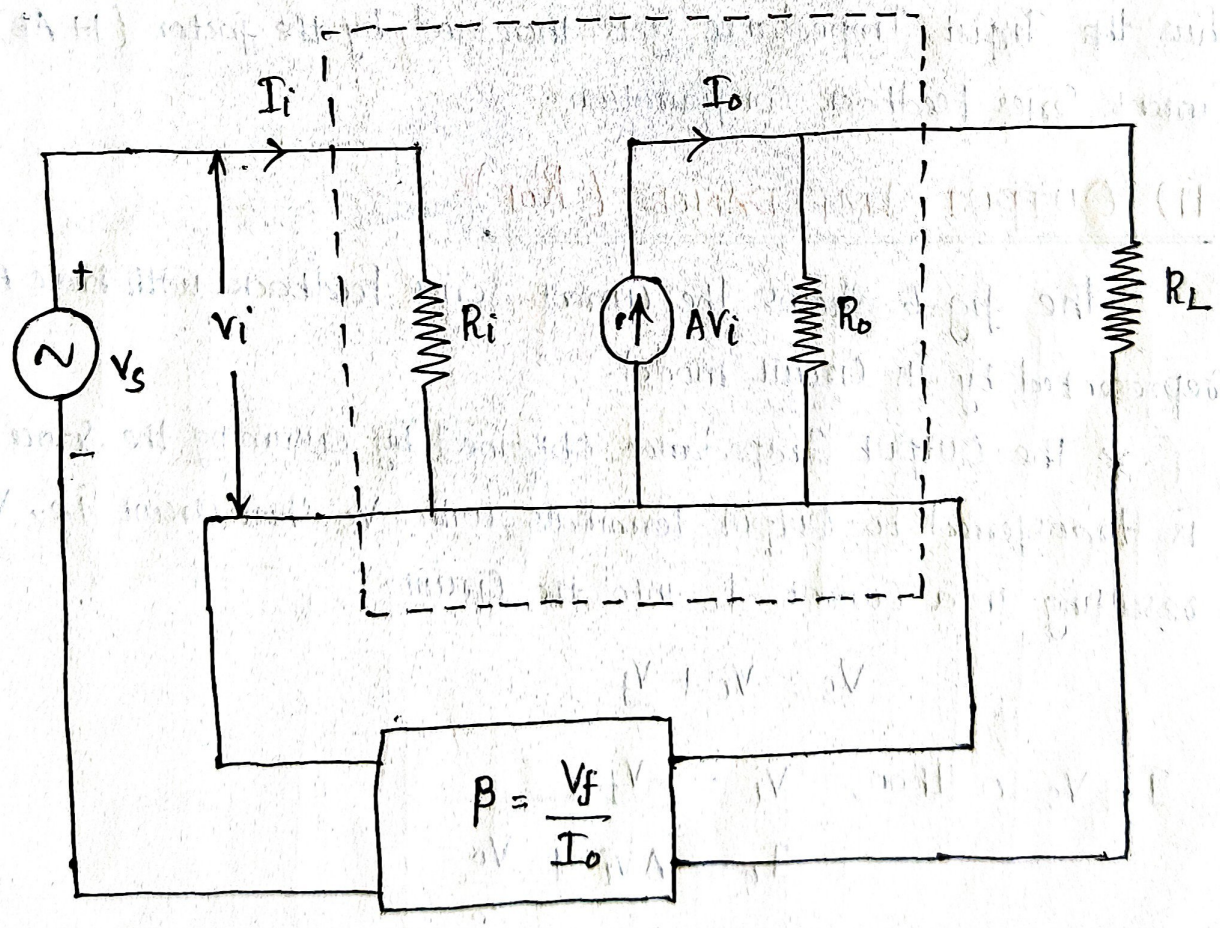


Fig. 6. Equivalent circuit of Current Series Feedback.

i) Input Impedance (R_{if})

From fig.6, $V_s = I_i R_i + V_f$

$= I_i R_i + \beta I_o$

$V_s = I_i R_i + \beta A V_i$

$I_o = A V_i$ $\qquad V_i = I_i R_i$

$\therefore V_s = I_i R_i + \beta A I_i R_i$

$V_s = I_i R_i (1 + A\beta)$

$\therefore R_{if} = \frac{V_s}{I_i} = \frac{I_i R_i (1+A\beta)}{I_i} = R_i (1+A\beta)$

$$\boxed{R_{if} = R_i (1+A\beta)}$$

Thus the Input Impedance gets increased by the factor $(1+A\beta)$ in Current Series Feedback Configuration.

ii) Output Impedance (R_{of})

The fig.6 shows the Current Series Feedback with basic Amplifier represented by its circuit model.

* The Output Impedance obtained by assuming the Source Voltage is transferred to Output terminals, with V_s short circuit i.e, $V_s = 0$, resulting in a Current I_o into the circuit.

$$V_s = V_i + V_f$$

If $V_s = 0$ then, $V_i = -V_f$

$$I_o = -A V_i + \frac{V_o}{Z_o}$$

$$= -A V_f + \frac{V_o}{Z_o}$$

$$I_o = -A\beta I_o + \frac{V_o}{Z_o}$$

$$I_o + A\beta I_o = \frac{V_o}{Z_o}$$

$$I_o (1 + A\beta) = \frac{V_o}{Z_o}$$

$$Z_o (1 + A\beta) = \frac{V_o}{I_o} = Z_{of} \text{ or } R_{of}$$

$$\therefore \boxed{R_{OF} = Z_o (1 + A\beta)}$$

Thus the Output Impedance of the Amplifier with feedback is increased by a factor of $(1 + A\beta)$

CURRENT SHUNT FEEDBACK

Fig. 7 shows the block diagram of Current Shunt Feedback. This case the output current is taken as feedback parameter and is fed in parallel with Input circuit. This is called as 'Current Shunt Feedback Configuration'.

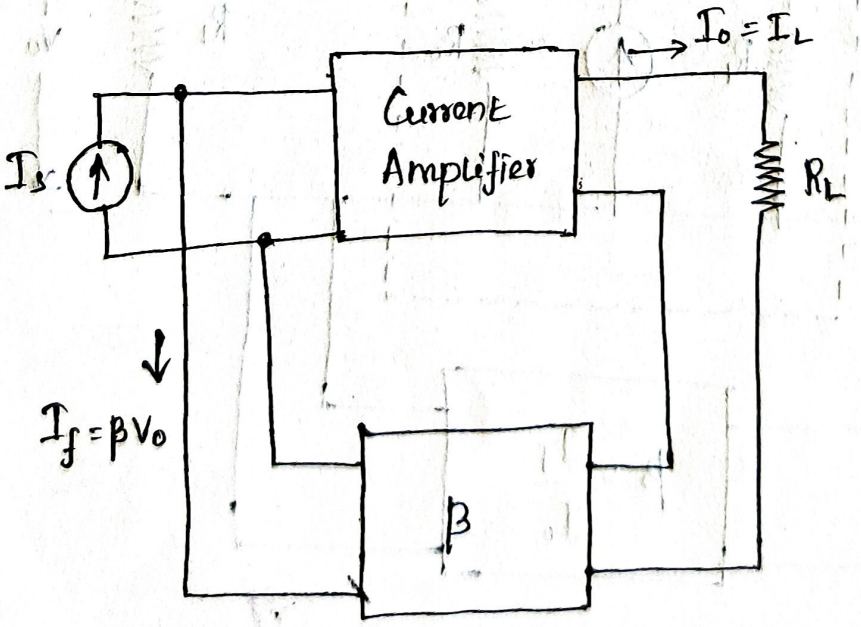


Fig. 7. Current Shunt Feedback

$A = \frac{V_o}{I_i}$ = Gain of Amplifier without Feedback.

$\beta = \frac{I_f}{I_o}$ = Feedback Factor

From the fig. 7, we know

$$I_s = I_i + I_f$$

$$I_f = \beta I_o \text{ and } I_o = A I_i$$

But the Gain of the Amplifier with Feedback

$$A_f = \frac{I_o}{I_s} = \frac{AI_i}{I_i + I_f} = \frac{A I_i}{I_i + \beta I_o} = \frac{A I_i}{I_i + \beta A I_i} = \frac{AI_i}{I_i(1+A\beta)}$$

$$\boxed{A_f = \frac{A}{1 \pm A\beta}}$$

Again the Gain with Feedback is seen to be reduced by a factor $(1+A\beta)$, when -ve Current Shunt Feedback is provided.

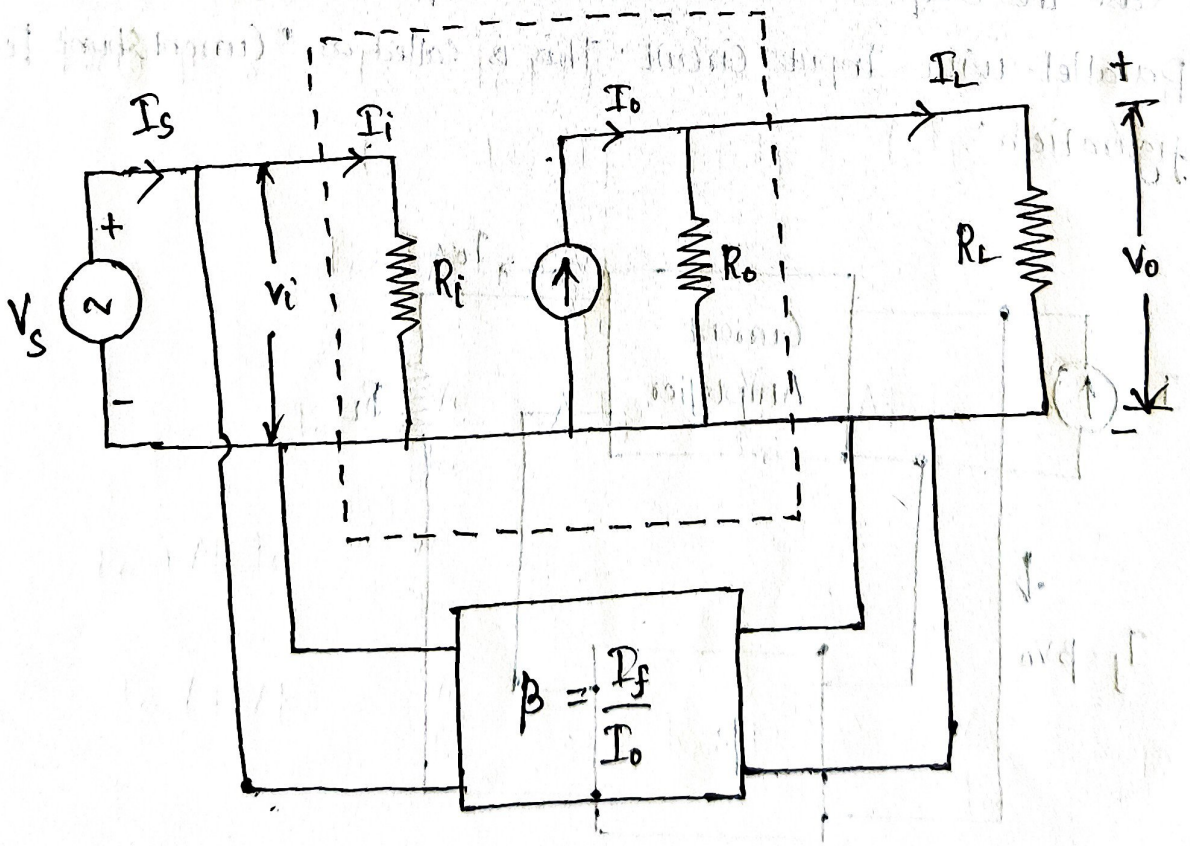


Fig. 8. Equivalent Circuit.

i) Input Impedance (R_{if})

From fig.8 $I_s = I_i + I_f$

$$= \frac{V_i}{R_i} + \beta I_o$$

$$= \frac{V_i}{R_i} + \beta A I_i$$

$$= \frac{V_i}{R_i} + \frac{\beta A V_i}{R_i}$$

$$I_s = \frac{V_i}{R_i}(1+A\beta)$$

$$R_{if} = \frac{V_i}{I_s} = \frac{V_i}{\frac{V_i}{R_i}(1+A\beta)}$$

$$\boxed{R_{if} = \frac{R_i}{1+A\beta}}$$

ii) Output Impedance (R_{of})

From fig.8 $I_s = I_i + I_f$

$$I_i = I_s - I_f = -I_f \quad (I_s = 0)$$

$$I_o = A I_i + \frac{V_o}{R_o}$$

$$I_o = \frac{V_o}{R_o} - A I_f = \frac{V_o}{R_o} - A\beta I_o$$

$$I_o + A\beta I_o = \frac{V_o}{R_o}$$

$$I_o(1+A\beta) = \frac{V_o}{R_o} \quad ; \quad R_o(1+A\beta) = \frac{V_o}{I_o} = R_{of}.$$

$$\boxed{R_{of} = R_o(1+A\beta)}$$

Thus the Output Impedance increased by $(1+A\beta)$.

UNIT-5

OSCILLATORS

Any circuit which is used to generate a periodic Voltage without an Ac Input Signal is called an 'Oscillator'.

- To generate the periodic Voltage, the circuit is Supplied with Energy from a dc Source. If the Output Voltage is a Sine wave function of time, the Oscillator is Called a 'Sinusoidal' or 'Harmonic' Oscillator.

* Positive Feedback and Negative Resistance Oscillators belong to this Category. There is another Category of Oscillators which generate 'Non-Sinusoidal Waveforms' Such as Square, Rectangular, Triangular or Saw tooth waves.

CONDITIONS FOR OSCILLATIONS (BARKHAUSEN CRITERION)

The Oscillator Circuit is Set into Oscillations by a Random Variation in the Base Current due to Noise Components or a Small Variation in the dc power Supply.

* The Noise Components i.e, extremely Small Random electrical Voltages and Currents are always present in any Conductor, tube or Transistor.

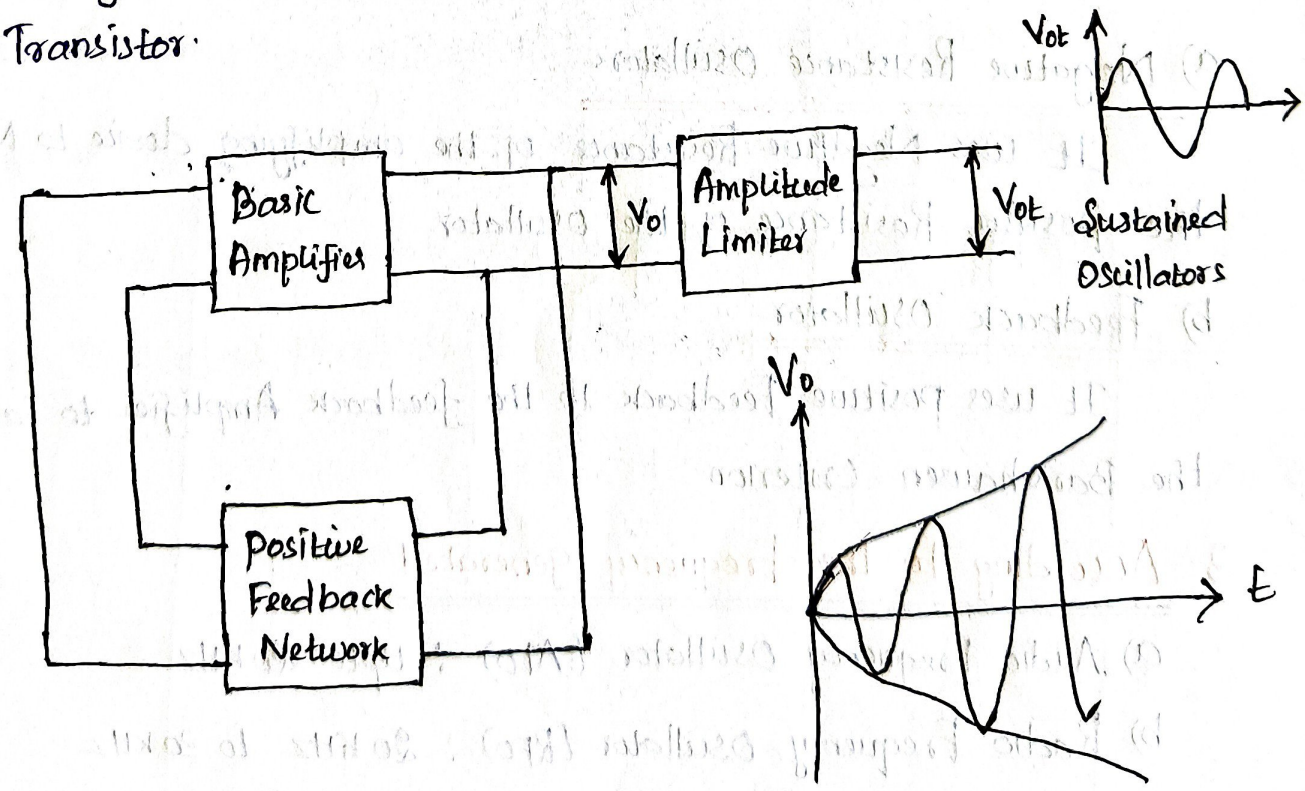


Fig. 1. Block diagram of an Oscillator.

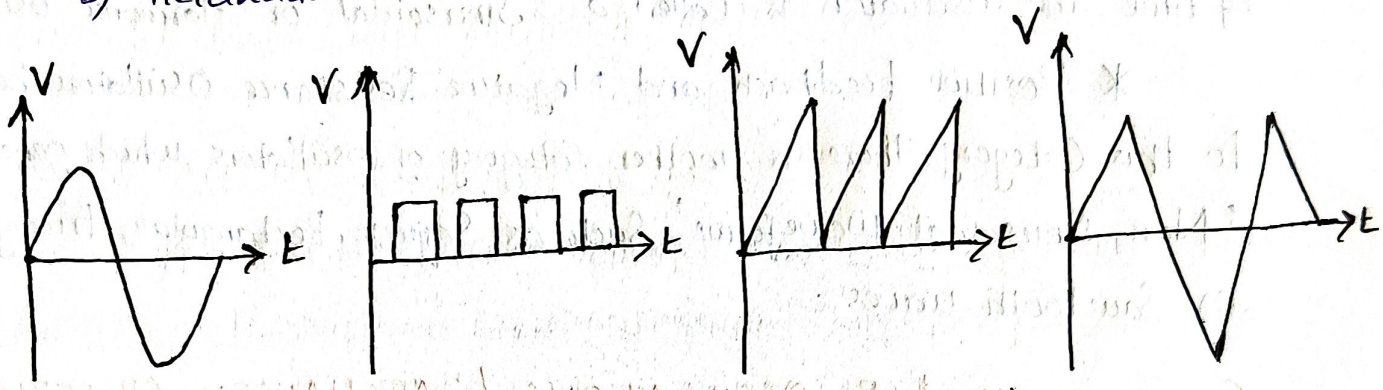
CLASSIFICATION OF OSCILLATORS

Oscillators are classified into the following ways

1. According to the waveforms generated

a) Sinusoidal Oscillator

b) Relaxation Oscillator



a) Sinusoidal b) Square c) Sawtooth d) Triangular

Fig. 2. Waveforms generated by Oscillators.

2. According to the fundamental Mechanisms Involved

a) Negative Resistance Oscillators

b) Feedback Oscillators

a) Negative Resistance Oscillators

It uses Negative Resistance of the amplifying device to Neutralize the positive Resistance of the Oscillator

b) Feedback Oscillator

It uses positive Feedback in the feedback Amplifier to satisfy the Barkhausen Criterion

3. According to the Frequency generated

a) Audio Frequency Oscillator (AFO) : upto 20 KHz

b) Radio Frequency Oscillator (RFO) : 20 KHz to 30 KHz

c) Very High Frequency oscillator (VHF) : 30 MHz to 300 MHz

d) Ultra High Frequency (UHF) Oscillator : 300 MHz to 3 GHz

e) Microwave Frequency Oscillator : above 3 GHz

4. According to the type of Circuit is used

Sine wave Oscillators may be classified as

a) LC tuned Oscillator

b) RC phase shift Oscillator.

MECHANISM FOR START OF OSCILLATIONS

If a small fraction (β) of the output signal is feedback to the Input with proper phase, relation then this feedback signal will be amplified by the Amplifier.

* If the Amplifier has a gain of more than $\frac{1}{\beta}$, then the Output Increases and thereby the Feedback Signal becomes larger. This process Continues and the Output goes on Increasing

– But as the Signal Level Increases the gain of the amplifier is reduced exactly equal to $\frac{1}{\beta}$. Then the Output Voltage remains constant at frequency f_o called 'Frequency of Oscillations'.

The Essential Conditions for maintaining Oscillations are

1. $|A\beta| = 1$ i.e., the magnitude of Loop Gain must be Unity.
2. The total phase shift around the Closed Loop is Zero or 360°.

HARTLEY OSCILLATOR

Hartley Oscillator shown in figure. 1, Z_1 and Z_2 are Inductors and Z_3 is a Capacitor

- Resistors R_1, R_2 and R_E Provide the necessary dc Bias to the Transistor.

- C_E is a bypass Capacitor, C_{C1} and C_{C2} are Coupling Capacitors. The Feedback Network Consisting of Inductors L_1 and L_2 and Capacitor C determines the Frequency of the Oscillator.

* When the Supply Voltage $+V_{CC}$ is Switched ON, a Transient Current is Produced in tank circuit and Consequently, damped harmonic Oscillations are Set up in the Circuit.

- The Oscillatory Current in the tank circuit Produces Ac Voltages across L_1 and L_2. As terminal 3 is earthed, it is at Zero Potential. If terminal '1' is at a positive potential with respect to '3' at any instant, terminal '2' will be at a Negative Potential with respect to '3' at Same Instant.

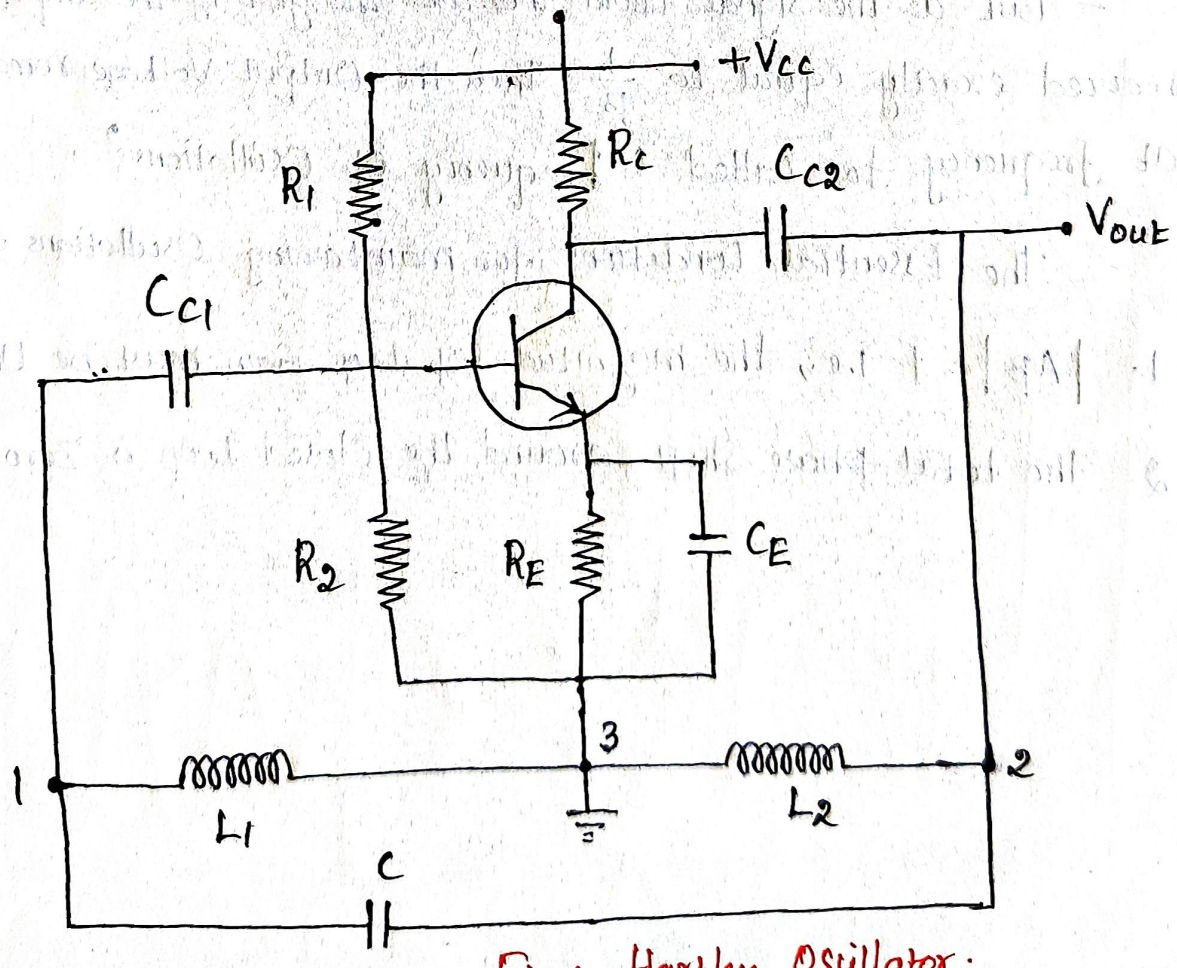


Fig. 1 Hartley Oscillator.

Thus the phase difference between the terminal 1 and 2 is always 180°. In the 'CE Mode' the transistor provides the phase difference of 180° between the Input and Output.

* Therefore the total phase shift is 360°. Thus at the Frequency determined for the tank circuit, the necessary condition for Sustained Oscillation is Satisfied.

- If the feedback is adjusted so that the Loop Gain $A\beta = 1$, the Circuit acts as an Oscillator.

The Frequency of Oscillation is

$$f_o = \frac{1}{2\pi\sqrt{LC}}$$

Where, $L = L_1 + L_2 + 2M$.

M - Mutual Inductance between the coils L_1 and L_2

The Condition for Sustained Oscillation is

$$h_{fe} \geq \frac{L_1 + M}{L_2 + M}$$

ANALYSIS

In the Hartley Oscillator Z_1 and Z_2 are Inductive Reactances and Z_3 is the Capacitive Reactance.

- If M is the Mutual Inductance between the Inductors, then

$$Z_1 = j\omega L_1 + j\omega M \quad ; \quad Z_1 = j\omega L_1$$

$$Z_2 = j\omega L_2 + j\omega M \quad ; \quad Z_2 = j\omega L_2$$

$$Z_3 = \frac{1}{j\omega C} = \frac{-j}{\omega C}$$

The general Equation for LC Oscillator is given by

$$h_{fe} Z_1 Z_2 + Z_3 Z_1 + Z_1 Z_2 + h_{ie}(Z_1 + Z_2 + Z_3) = 0.$$

$$h_{fe}(j\omega L_1)(j\omega L_2) + \left(\frac{-j}{\omega C}\right)(j\omega L_1) + (j\omega L_1)(j\omega L_2) + h_{ie}\left(j\omega L_1 + j\omega L_2 - \frac{j}{\omega C}\right) = 0$$

$$-h_{fe}\omega^2 L_1 L_2 + \frac{L_1}{C} - \omega^2 L_1 L_2 + h_{ie} j\omega \left[L_1 + L_2 - \frac{1}{\omega^2 C}\right] = 0$$

To determine the Frequency of oscillations, the imaginary part is equated to Zero. i.e, $\omega h_{ie}\left(L_1 + L_2 - \frac{1}{\omega^2 C}\right) = 0$

$$L_1 + L_2 = \frac{1}{\omega^2 C}$$

$$\omega^2 = \frac{1}{(L_1+L_2)C} \quad ; \quad \omega = \frac{1}{\sqrt{(L_1+L_2)C}}$$

$$f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi\sqrt{(L_1+L_2)C}} = \frac{1}{2\pi\sqrt{L_{eq}\cdot C}}$$

$$\boxed{f_0 = \frac{1}{2\pi\sqrt{L_{eq}\cdot C}}} \qquad (L_{eq} = L_1 + L_2)$$

To determine the conditions for oscillation the real part is equated to Zero

$$-h_{fe}\omega^2 L_1 L_2 + \frac{L_1}{C} - \omega^2 L_1 L_2 = 0$$

$$\omega^2 L_1 L_2 (1 + h_{fe}) - \frac{L_1}{C} = 0$$

$$\frac{L_1}{C} = \omega^2 L_1 L_2 (1 + h_{fe})$$

Substitute ω^2 value

$$\frac{L_1}{C} = \frac{L_1 L_2 (1+h_{fe})}{(L_1+L_2)C} \Rightarrow \frac{L_1 L_2}{L_1+L_2}(1+h_{fe}) = L_1$$

$$1 + h_{fe} = \frac{L_1(L_1+L_2)}{L_1 L_2} \Rightarrow 1 + h_{fe} = \frac{L_1+L_2}{L_2}$$

$$1 + h_{fe} = \frac{L_1}{L_2} + \frac{L_2}{L_2} \Rightarrow 1 + h_{fe} = 1 + \frac{L_1}{L_2} \quad \therefore \boxed{h_{fe} = \frac{L_1}{L_2} = \beta}$$

Thus the Condition for the sustained Oscillation.

COLPITS OSCILLATOR

The Colpits Oscillator shown in figure. 1.

Z_1 and Z_2 are Capacitors and Z_3 is an Inductor. The resistors R_1, R_2 and R_E provide the Necessary dc bias to the Transistor &

* C_E is a bypass Capacitor. C_{C1} and C_{C2} are Coupling Capacitors. The Feedback Network Consisting of Capacitors C_1 and C_2 and an Inductor L determines the 'Frequency of Oscillation'.

– When the Supply Voltage $+V_{CC}$ is Switched ON, a transient Current is produced in the tank circuit and Consequently, damped harmonic Oscillations are Setup in the Circuit.

• The Oscillatory Current in the tank circuit Produces AC voltage across C_1 and C_2. As terminal 3 is earthed, it will be at zero potential If the terminal 1 is at a positive potential with respect to '3' at any instant, terminal 2 will be at a Negative Potential with respect to '3' at the same Instant

– Thus the phase difference between terminals, '1' and '2' is always 180°. In the CE mode, the transistor provides the phase difference of 180° between the Input and Output. Therefore the total Phase Shift is 360°

* Thus at the frequency determined for the tank circuit, the necessary condition for Sustained Oscillations is Satisfied. If the Feedback is adjusted so that the Loop Gain $A\beta = 1$, the Circuit acts as an Oscillator.

The Frequency of Oscillation is

$$\boxed{f_o = \frac{1}{2\pi\sqrt{LC}}}$$

Where, $\frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2}$ i.e, $C = \frac{C_1 C_2}{C_1 + C_2}$.

It is widely used in commerical signal generators for frequencies between 1 MHz and 500 MHz. It is also used as a Local Oscillator in Super heterodyne Radio Receiver.

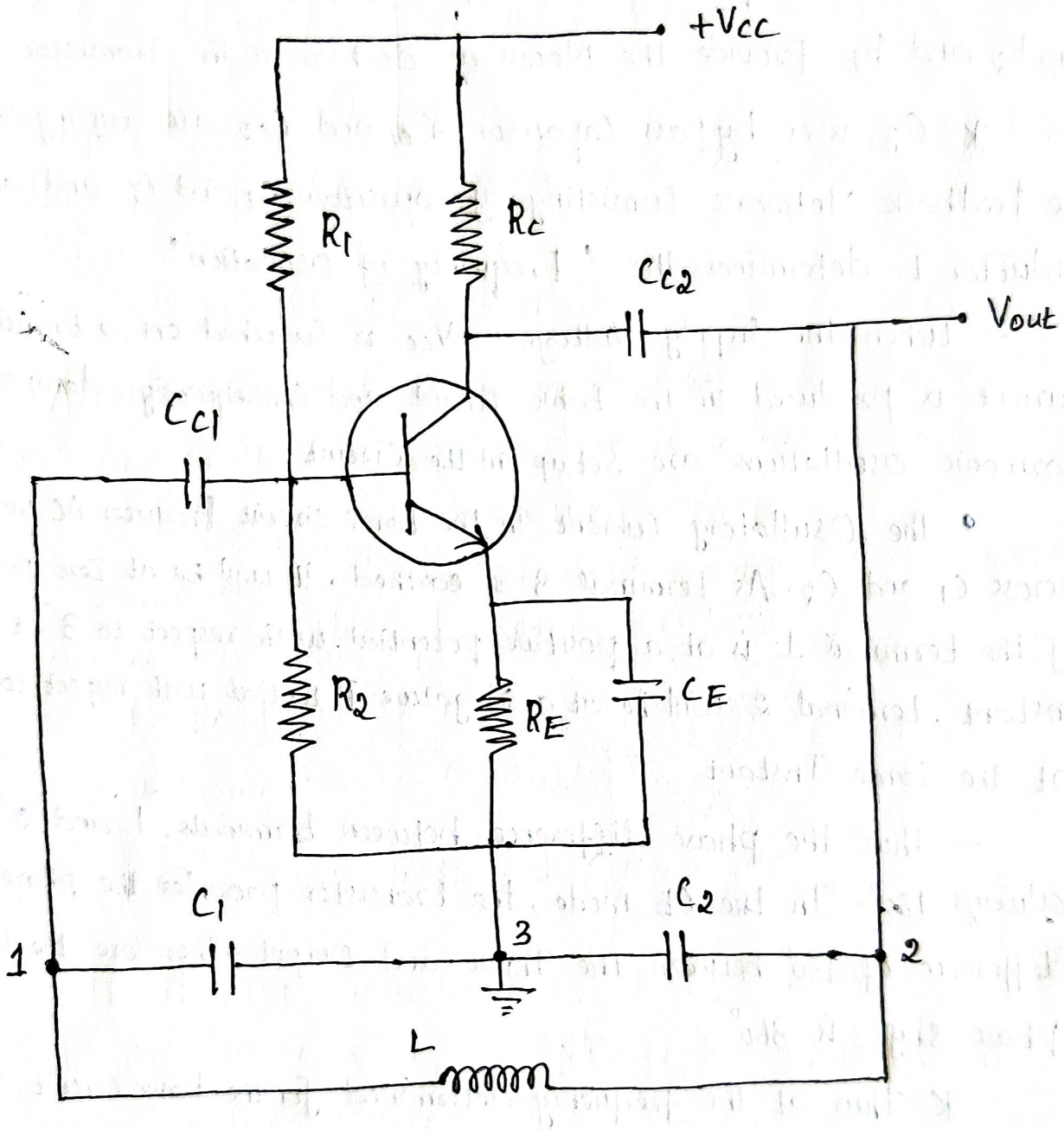


Fig.1. Colpitt's Oscillator

ANALYSIS

For this Oscillator, $Z_1 = \frac{1}{j\omega C_1} = \frac{-j}{\omega C_1}$

$Z_2 = \frac{1}{j\omega C_2} = \frac{-j}{\omega C_2}$

$Z_3 = j\omega L$

The general Equation for LC Oscillator

$$h_{fe} Z_1 Z_2 + Z_3 Z_1 + Z_1 Z_2 + h_{ie}(Z_1 + Z_2 + Z_3) = 0.$$

$$h_{fe}\left(\frac{-j}{\omega C_1}\right)\left(\frac{-j}{\omega C_2}\right) + (j\omega L)\left(\frac{-j}{\omega C_1}\right) + \left(\frac{-j}{\omega C_1}\right)\left(\frac{-j}{\omega C_2}\right) + h_{ie}\left(\frac{-j}{\omega C_1} + \frac{-j}{\omega C_1} + j\omega L\right) = 0$$

$$-h_{fe}\frac{1}{\omega^2 C_1 C_2} + \frac{L}{C_1} - \frac{1}{\omega^2 C_1 C_2} + h_{ie}\left(\frac{-j}{\omega C_1} - \frac{j}{\omega C_2} + j\omega L\right) = 0$$

$$-h_{fe}\frac{1}{\omega^2 C_1 C_2} + \frac{L}{C_1} - \frac{1}{\omega^2 C_1 C_2} + j h_{ie}\left(\frac{-1}{\omega C_1} - \frac{1}{\omega C_2} + j\omega L\right) = 0$$

To determine the Frequency of Oscillations equate the Imaginary Part of Zero.

$$h_{ie}\left(\frac{-1}{\omega C_1} - \frac{1}{\omega C_2} + \omega L\right) = 0$$

$$-\frac{1}{\omega C_1} - \frac{1}{\omega C_2} + \omega L = 0$$

$$\omega L = \frac{1}{\omega C_1} + \frac{1}{\omega C_2}$$

where,

$$\omega^2 L = \frac{1}{C_1} + \frac{1}{C_2} \qquad \frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2}$$

$$\omega^2 = \frac{1}{C_{eq} L}$$

$$\omega = \frac{1}{\sqrt{C_{eq} L}}$$

$$f_0 = \frac{\omega_0}{2\pi}$$

$$\boxed{f_0 = \frac{1}{2\pi\sqrt{C_{eq} L}}}$$

To determine the condition for Oscillation, Real part is equated to zero

$$-h_{fe}\frac{1}{\omega^2 C_1 C_2} + \frac{L}{C_1} - \frac{1}{\omega^2 C_1 C_2} = 0$$

Substituting this value and simplifying, we get

$$\boxed{h_{fe} = \frac{C_2}{C_1}}$$

Thus the Condition for the Sustained Oscillation.

RC OSCILLATORS

All the Oscillators using Tuned LC circuits operates well at high frequencies. At Low frequencies, as the Inductors and Capacitors required for the time circuit would be very Bulky.

- Rc Oscillators are found to be more Suitable. Two important Rc Oscillators are

i) Rc phase shift Osillator

ii) Wien Bridge Osillator

RC PHASE SHIFT OSCILLATOR

In this Oscillator, the required phase shift of 180° in the Feedback loop from Output to Input is obtained by using 'R' and 'C' components Instead of tank circuit.

* Rc phase shift Oscillator basically consists of an Amplifier and a feedback Network in 'Ladder Fashion' hence such an Oscillator is also called 'Ladder type Rc phase shift Oscillator'.

RC FEEDBACK NETWORK :

The Rc Network is used in Feedback Path. In Oscillator Feedback, Network must introduce a phase shift of 180° to obtain total phase shift around a loop as 360°.

Thus if one RC Network produces phase shift of $\phi = 60^\circ$, then to Produce phase shift of 180° such three RC Network must be connected in cascade.

* Hence RC phase shift Oscillator with the feedback Network Consists of three RC Selections, each producing a phase shift of 60° thus the total phase shift due to feedback is 180° (360°).

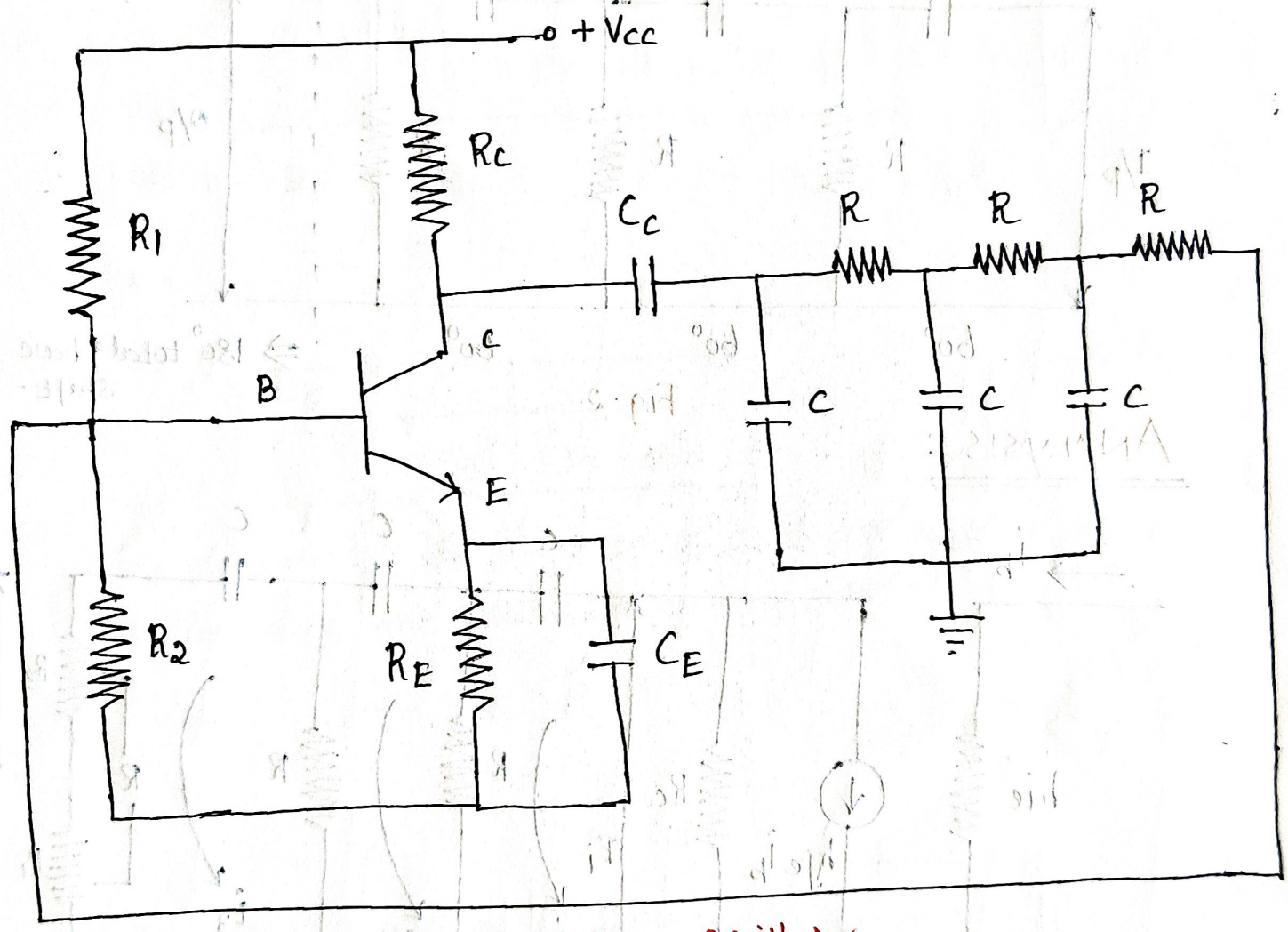


Fig. 1. RC Phase shift Oscillator.

The Network is also called the Ladder Network. All the Resistance Values and all the Capacitance Values are same, so that for a particular Frequency, each selection of R and C produces a phase shift of 60°.

- The frequency of oscillation is given by.

$$f_0 = \frac{1}{2\pi RC\sqrt{6}}$$

At this frequency, it is found that the feedback factor of the Network is $|\beta| = 1/29$.

- In order that $|A\beta|$ shall not be less than Unity, it is required that the Amplifier Gain $|A|$ must be more than 29 for oscillator operation.

* The RC phase shift Oscillator is suitable for Audio frequencies only.

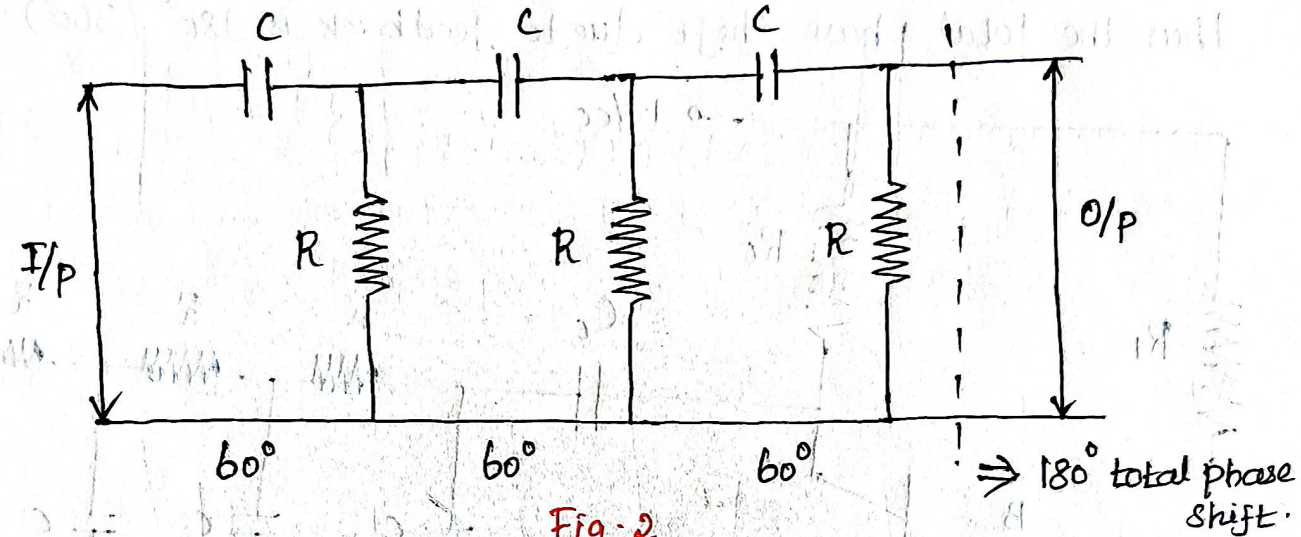


Fig. 2

ANALYSIS :

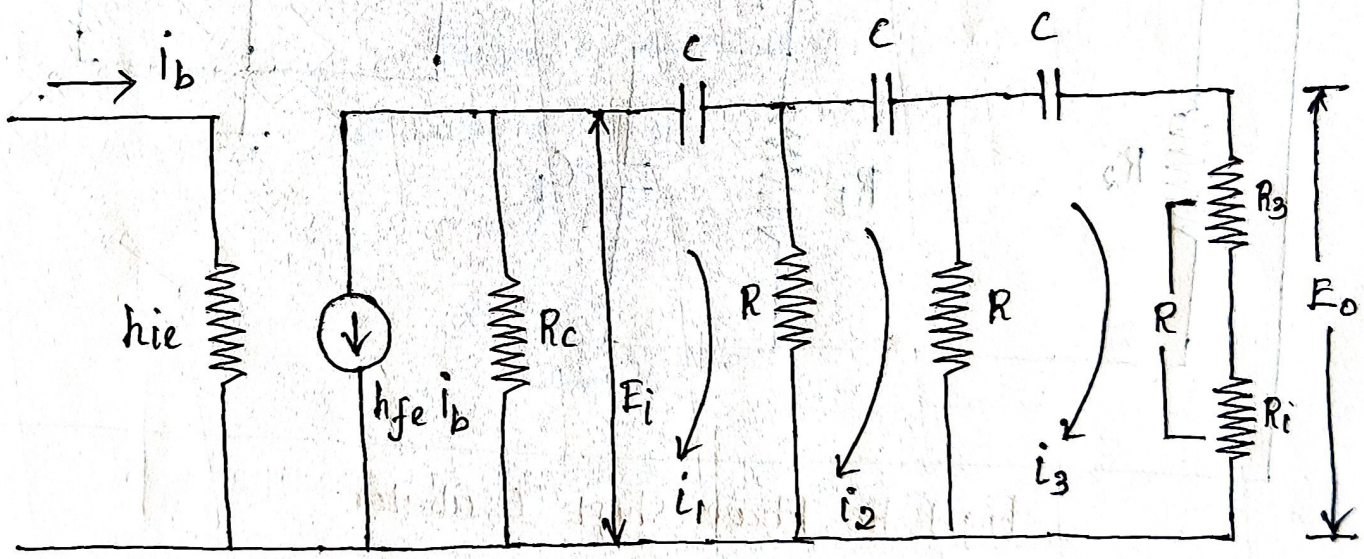


Fig. 3. Equivalent Circuit.

From fig. 3, we can write the following three equations:

$$I_1\left(R + \frac{1}{j\omega C}\right) - I_2 R = E_i$$

$$-I_1 R + I_2\left(2R + \frac{1}{j\omega C}\right) - I_3 R = 0$$

$$-I_2 R + I_3\left(2R + \frac{1}{j\omega C}\right) = 0$$

Solving the above simultaneous equations, we get

$$I_3 = \frac{Ei}{R}\left[\frac{1}{(1-5\alpha^2)+j\alpha(\alpha^2-6)}\right]$$

where, $\alpha = \frac{1}{\omega CR}$

$$E_0 = Ei\left[\frac{1}{(1-5\alpha^2)+j\alpha(\alpha^2-6)}\right]$$

where, $E_0 = I_3 R$ & $Ei = A \cdot R$

Hence $\beta = \frac{E_0}{Ei}$

$$\beta = \frac{1}{(1-5\alpha^2)+j\alpha(\alpha^2-6)}$$

For determining the frequency of oscillation the phase shift, i.e, the imaginary part must be equal to zero.

Hence, $\alpha(\alpha^2-6) = 0$

$$\alpha = \frac{1}{\omega_0 CR}\sqrt{6}$$

∴ The frequency of oscillation $f_0 = \frac{1}{2\pi RC\sqrt{6}}$

The condition for maintanence of oscillation is obtained by substituting $\alpha = \sqrt{6}$ into β thus, we get

$$\beta = -\frac{1}{29}$$

$$\beta = \frac{1}{29}\angle 180^\circ$$

$\beta = \frac{1}{A}$

$A = 29$

As per the Barkhausen Criterion to produce the sustained oscillation.

WEIN BRIDGE OSCILLATOR

The Circuits Consists of a two stage RC coupled Amplifier which provides a phase shift of 360° or 0°.

- A Balanced Bridge is used as the feedback Network which has No Need to provide any additional phase shift.

* The Feedback Network Consists of a lead-lag Network (R_1-C_1 and R_2-C_2) and a Voltage divider (R_3-R_4). The Lead Lag Network provides a positive Feedback to the Input of the First stage and the Voltage divider provides a Negative Feedback to the Emitter of Q_1.

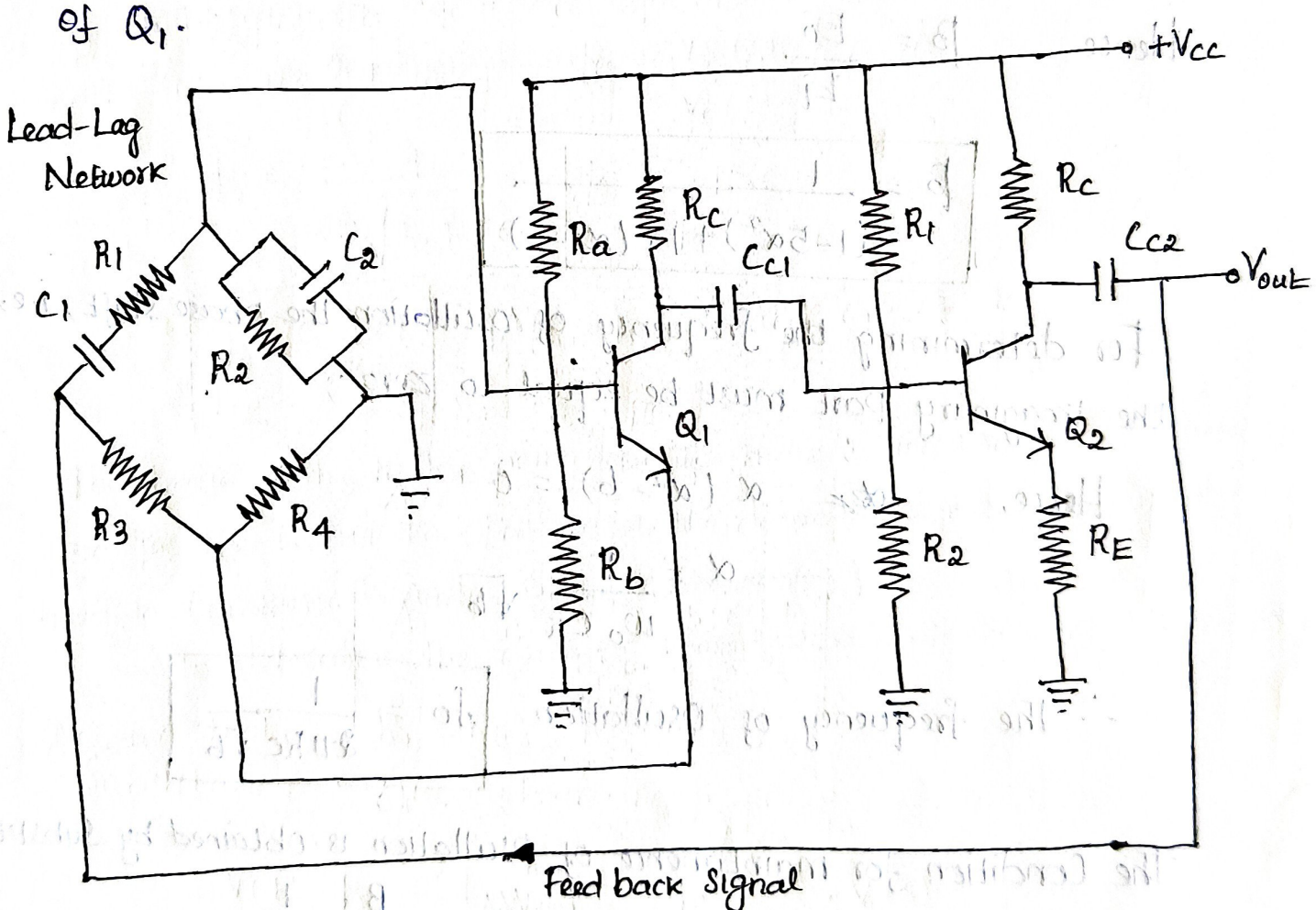


Fig.1. Wein Bridge Oscillator

If the bridge is balanced, $$\frac{R_3}{R_4} = \frac{R_1 - jX_{C1}}{\left[\frac{R_2(-jXC_2)}{R_2 - jXC_2}\right]} \quad \text{—— (1)}$$

where, X_{C1} and X_{C2} are the Reactance of the capacitors.

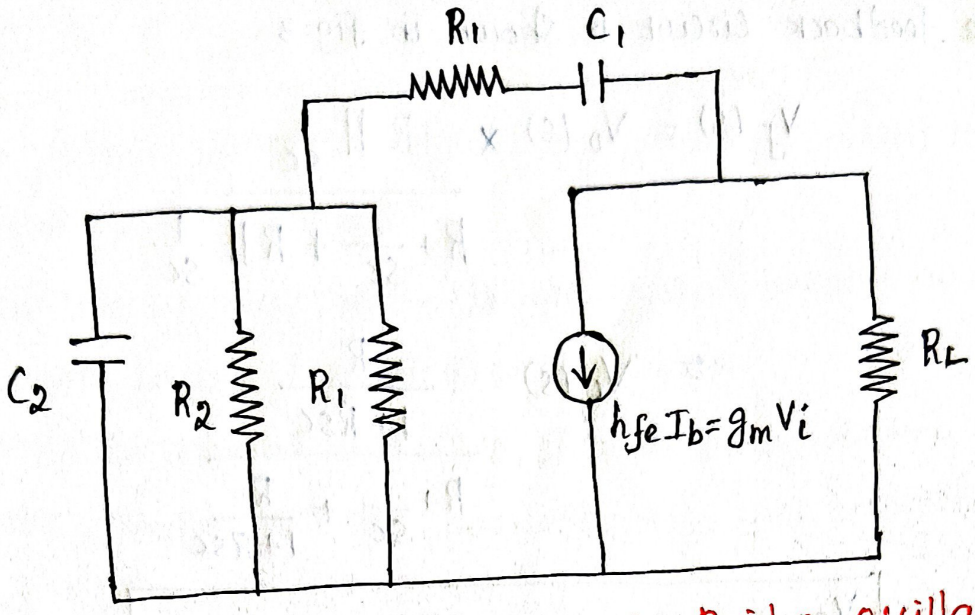


Fig. 2. Equivalent circuit of wein's Bridge Oscillator.

By simplifying the eqn ① and equating the Real and Imaginary Parts on both sides, we get the frequency of oscillations as,

$$f_r = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

$$\boxed{f_r = \frac{1}{2\pi RC}}, \text{ if } R_1 = R_2 = R \text{ and } C_1 = C_2 = C$$

The Ratio of R_3 to R_4 being greater than 2 will provide a Sufficient gain for the circuit to Oscillate at the desired frequency. This Oscillator is used in Commerical Audio Signal Generators.

– To determine the Gain of Wein Bridge Oscillator using BJT Amplifier,

Assume that $R_1 = R_2 = R$ and

$C_1 = C_2 = C$

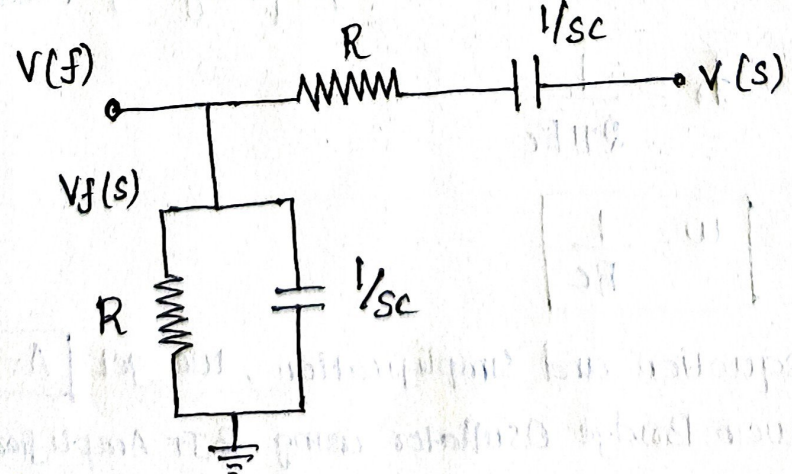


Fig. 3. Feed back circuit

Then the feedback circuit is shown in fig.3.

Therefore $$V_f(s) = V_0(s) * \frac{R \,||\, \frac{1}{sC}}{R + \frac{1}{sC} + R \,||\, \frac{1}{sC}}$$

$$= V_0(s) \frac{\frac{R}{1+RSC}}{R + \frac{1}{sC} + \frac{R}{1+RSC}}$$

$$\boxed{V_f(s) = V_0(s) \frac{sRSC}{R^2s^2C^2 + 3RSC + 1}}$$

Hence the Feedback Factor is $\beta = \frac{V_f(s)}{V_0(s)}$

$$\boxed{\beta = \frac{RSC}{R^2s^2C^2 + 3RSC + 1}}$$

We know that $A\beta = 1$

Therefore the Gain of the Amplifier

$$A = \frac{1}{\beta}$$

$$\boxed{A = \frac{R^2s^2C^2 + 3RSC + 1}{RSC}}$$

Substituting $S = j\omega$, where the frequency of Oscillation

$$f_r = \frac{1}{2\pi RC}$$

$$\boxed{\omega = \frac{1}{RC}}$$

the above equation and simplification, we get $\boxed{A = 3}$. Hence the gain of the Wein Bridge Oscillator using BJT Amplifier is atleast equal to 3 for Oscillations to occur.

CRYSTAL OSCILLATORS

Here it is a Colpitts Crystal Oscillators in which the Inductor is replaced by the 'Crystal'.

- In this type a piezo-electric Crystal, usually quartz is used as a Resonant Circuit replacing an LC Circuit.

* The Crystal is a thin slice of Piezo-electric material, such as quartz, Tourmaline and Rochelle salt, which exhibit a property Called 'piezo-electric Effect'.

- The piezo electric effect represents the characteristics that the Crystal reacts to any Mechanical stress by Producing an electric charge. In the Reverse Effect, an electric field results in Mechanical Strain.

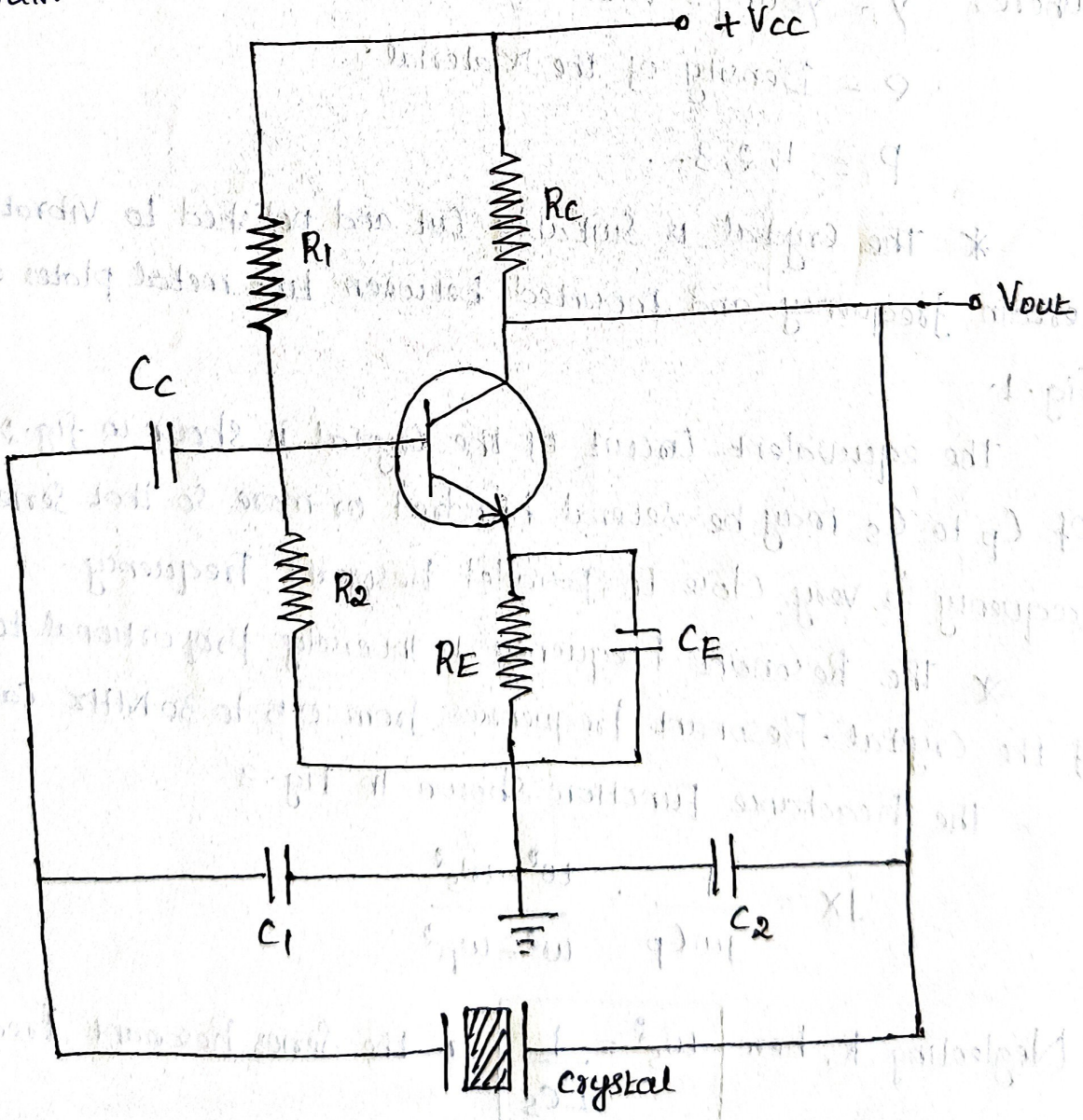


Fig.1. Colpitts Crystal Oscillator

If an alternating voltage is applied, then the crystal wafer is set into vibration. The frequency of vibration equal to the Resonant frequency of the crystal is determined by its structural characteristics.

- If the frequency of the applied AC voltage is equal to the Natural Resonant frequency of the crystal, then the maximum amplitude of vibration will be obtained.

* In general, the frequency of vibration is inversely proportional to the thickness of the crystal

The frequency of vibration is

$$f = \frac{P}{2l}\sqrt{\frac{Y}{\rho}}$$

Where, Y - Young's Modulus

ρ - Density of the Material.

$P = 1, 2, 3 \ldots$

* The crystal is suitably cut and polished to vibrate at a certain frequency and mounted between two metal plates as shown in fig. 1.

The equivalent circuit of the crystal is shown in fig. 2. The Ratio of C_p to C_s may be several hundred or more so that series Resonance frequency is very close to parallel Resonant frequency.

* The Resonant Frequency is inversely proportional to the thickness of the crystal. Resonant frequencies from 0.5 to 30 MHz can be obtained

- The Reactance function shown in fig. 3.

$$jX = \frac{1}{j\omega C_p} \cdot \frac{\omega^2 - \omega_s^2}{\omega^2 - \omega_p^2}$$

Neglecting R, here $\omega_s^2 = \frac{1}{LC_s}$ is the series Resonant Frequency

$$\omega_p^2 = \frac{1}{L\left[\frac{1}{C_S} + \frac{1}{C_P}\right]}$$ is the Parallel Resonant Frequency.

Since $C_P >> C_S$, $\omega_p = \omega_s$.

For $\omega_s < \omega < \omega_p$, the reactance is inductive and for ω out of the above range, it is capacitive

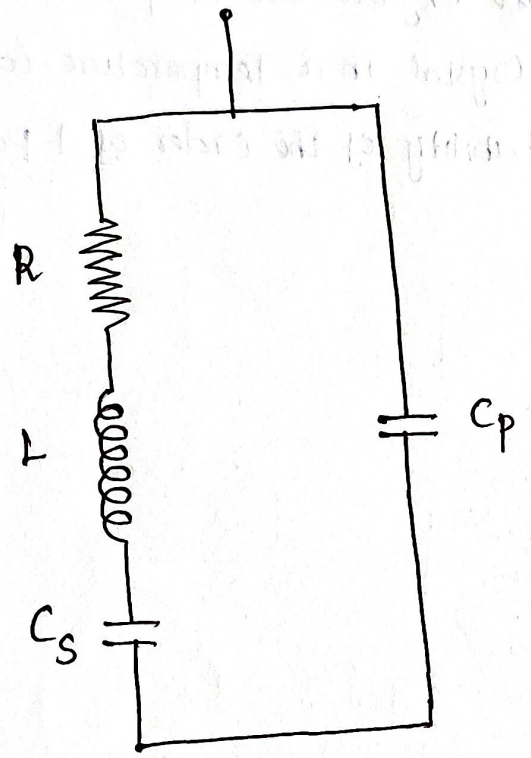


Fig.2. Electrical Equivalent Circuit.

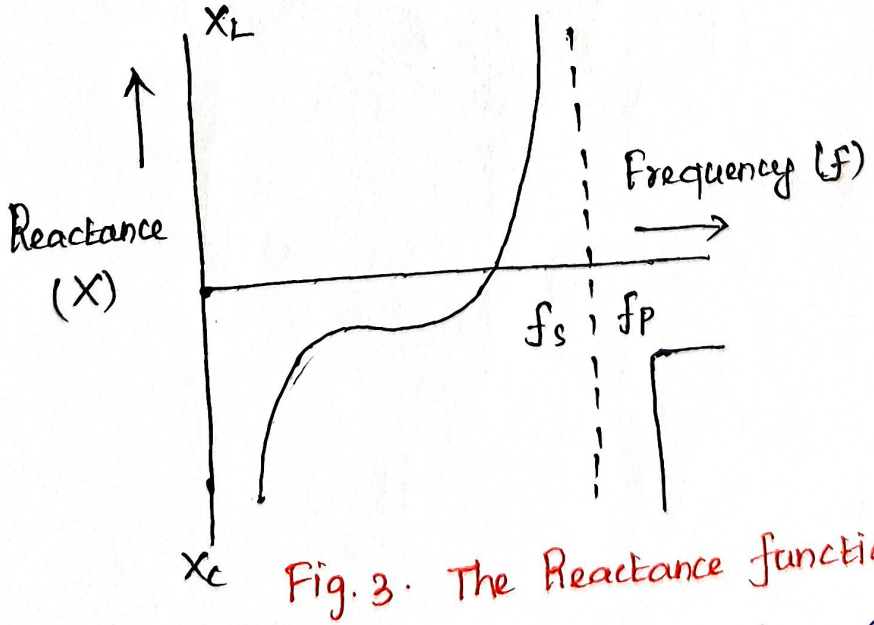


Fig. 3. The Reactance function when R = 0

For Crystal Hartley Osiellator, the capacitors C_1 and C_2 shown in fig. are replaced with inductors L_1 and L_2 respectively, so that the Reactance of the Crystal is capacitive

Hence, its Oscillation frequency is

$$= \frac{1}{2\pi\sqrt{(L_1+L_2)C}}$$

The advantage of the crystal is its very high Q as a Resonant circuit, which results in good frequency stability for the Oscillator. However, since the Resonant frequency of the crystals are temperature dependent, it is Necessary to enclose the crystal in a Temperature Controlled oven to achieve the frequency stability of the order of 1 part in 10^{10}.